



LVS
of CMOS
Inverter
and
2-input NAND
continuation-2

Aim:

To understand the basics of
KLayout's LVS

Disclaimer:

This document is for personal records only.
There is NO WARRANTY on technical
correctness.



By Kazzz-S (2023-03-08)
con-1 (2023-03-01)
original (2023-02-21)

Part-VI: Errata

In LVS-CMOS-Inverter-NAND.pptx

13. Using DMOS4 for the **inv.cir** Tutorial

2. Prepare four SPICE deck files to test all S and D combinations.

```
1 |
2 * Simple CMOS inverter circuit: original: (PMOS, NMOS)=(incorrect, correct)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
6 Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
```

\$choice=1

D and S are swapped

```
1 |
2 * Simple CMOS inverter circuit: Variant X1: (PMOS, NMOS)=(incorrect, incorrect)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
6 Mn VSS IN OUT SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
9
```

\$choice=2

```
1 |
2 * Simple CMOS inverter circuit: Variant X2: (PMOS, NMOS)=( correct, incorrect)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 Mp OUT IN VSS NWELL PMOS W=1.5U L=0.25U
6 Mn VSS IN OUT SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
9
```

\$choice=3

This should have been "VDD"

```
1 |
2 * Simple CMOS inverter circuit
3
4 * Original: ${klayout_root}/testdata/lvs/inv.cir
5
6 * Modified: inv-DMOS4.cir (PMOS, NMOS)=( correct, correct) $choice=4
7 * by: Kazzz-S
8 * date: 2023-02-16
9 * aims: 1) correct D-S connections of the PMOS (flipped in the original)
10
11 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
12 * Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
13 Mp OUT IN VDD NWELL PMOS W=1.5U L=0.25U
14 Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U
15 .ENDS
16
```

I expect this should match!

Sorry for the inconvenience caused.

In LVS-CMOS-Inverter-NAND-Con1.pptx

17. Using DMOS4 for the **inv.cir** Tutorial

2. Prepare four SPICE deck files to test all S and D combinations.

```
1 |
2 * Simple CMOS inverter circuit : original: (PMOS, NMOS)=(incorrect, correct)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
6 Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
```

\$choice=1

D and S are swapped

```
1 |
2 * Simple CMOS inverter circuit: Variant X1: (PMOS, NMOS)=(incorrect, incorrect)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
6 Mn VSS IN OUT SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
9
```

\$choice=2

```
1 |
2 * Simple CMOS inverter circuit: Variant X2: (PMOS, NMOS)=( correct, incorrect)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 Mp OUT IN VSS NWELL PMOS W=1.5U L=0.25U
6 Mn VSS IN OUT SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
9
```

\$choice=3

This should have been "VDD"

```
1 |
2 * Simple CMOS inverter circuit
3
4 * Original: ${klayout_root}/testdata/lvs/inv.cir
5
6 * Modified: inv-DMOS4.cir (PMOS, NMOS)=( correct, correct)
7 * by: Kazzz-S
8 * date: 2023-02-16
9 * aims: 1) correct D-S connections of the PMOS (flipped in the original)
10
11 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
12 * Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
13 Mp OUT IN VDD NWELL PMOS W=1.5U L=0.25U
14 Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U
15 .ENDS
16
```


\$choice=4

I expect this should match!

Sorry for the inconvenience caused.

Part-VII: Re-experiments with MOS4

20. Test Environment



About KLayout

KLayout 0.28.5

By Matthias Köfferlein, Munich 2023-03-06 r7a31c2abf

For feedback and bug reports mail to: contact@klayout.de

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Build options:

- Ruby interpreter 3.1.3-p185 (x86_64-linux)
- Python interpreter 3.8.10 (default, Nov 14 2022, 12:59:47) [GCC 9.4.0]
- Qt bindings for scripts


Binary extensions:

MK

Commit [87e2def2](#) (open)
by [Matthias Köfferlein](#), 2023-03-05 06:38
parent [feb50f49](#)
child [7a31c2ab](#)


Include version folder in python module sources

branches master-upstream, upstream/master
merged to branches [master](#), [master-mac-qt6](#), [origin/master](#), [origin/master-mac-qt6](#)

Spice netlist reader: should read "M" terminals in DGS order. #1304

Open

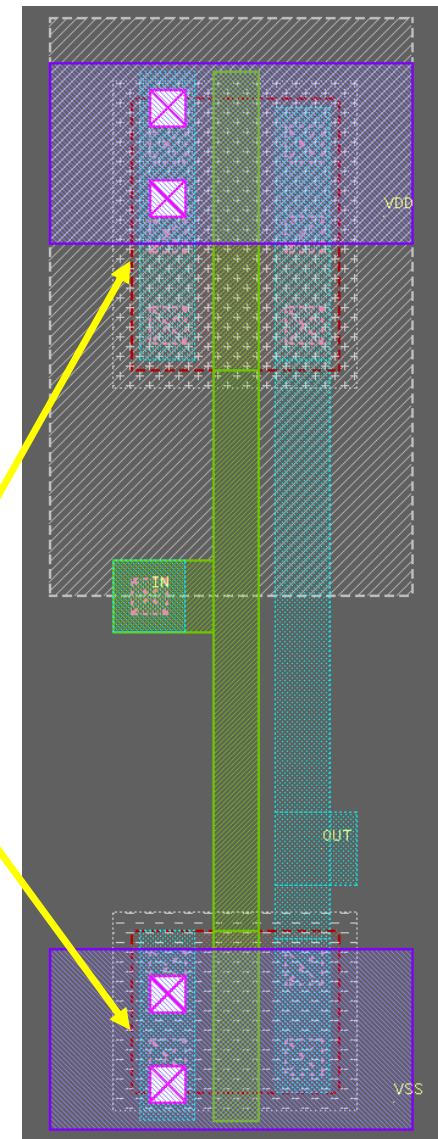
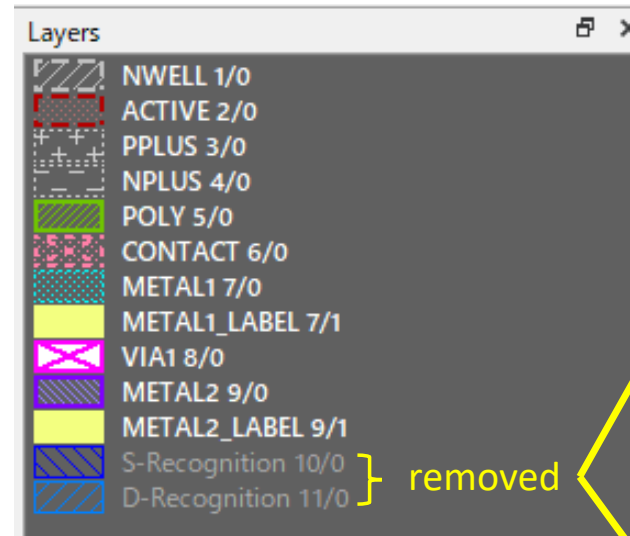
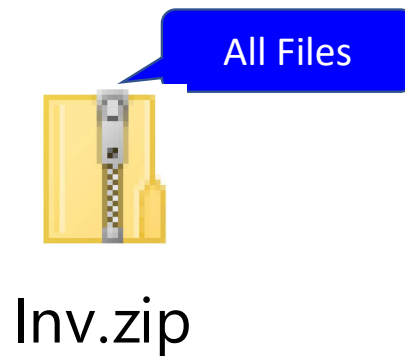
klayoutmatthias opened this issue last week · 0 comments

 Merge pull request [#1305](#) from KLayout/issue-1304

Close

21. Using MOS4 for the **inv.cir** Tutorial

1. Remove the two dummy layers for S- and D-recognition that were added to use the DMOS4 extractor.



21. Using MOS4 for the **inv.cir** Tutorial

2. Prepare four SPICE deck files to test all S and D combinations.

```
1
2 * Simple CMOS inverer circuit : original: (PMOS, NMOS)=(incorrect, correct)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
6 Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
```

\$choice=1

D and S are swapped

```
1
2 * Simple CMOS inverer circuit Variant X1: (PMOS, NMOS)=(incorrect, incorrect)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
6 Mn VSS IN OUT SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
```

\$choice=2

```
1
2 * Simple CMOS inverer circuit Variant X2: (PMOS, NMOS)=( correct, incorrect)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 Mp OUT IN VDD NWELL PMOS W=1.5U L=0.25U
6 Mn VSS IN OUT SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
```

\$choice=3

```
1
2 * Simple CMOS inverter circuit
3 *
4 * Original: ${layout_root}/testdata/lvs/inv.cir
5 *
6 * Modified: inv-correct.cir PMOS, NMOS)=( correct, correct)
7 * by: Kazzzz-S
8 * date: 2023-03-06
9 * aims: 1) correct D-S connections of the PMOS (flipped in the original)
10
11 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
12 * Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
13 Mp OUT IN VDD NWELL PMOS W=1.5U L=0.25U
14 Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U
15 .ENDS
16
```

\$choice=4

I expect all four should match by S-D swapping.

21. Using MOS4 for the **inv.cir** Tutorial

3. Modify the sample LVS script for testing and debugging.

```
46         exit
47     when 1, 2, 3, 4
48         @spicedeck = [ $choi
49     else
50         puts "### Usage [ 0=
51         puts "        Set one
52         puts "        then, ex
53         return
54     end
55 end
56 end
57 end
58
59 #-----
60 # [1] Design
61 #-----
62 dirName, baseName = File.spl
63 Dir.chdir(dirName)
64
65 source( "inv.oas", "INVERTER
66
67 deep
68
69 selector = SpiceDeckSelector
70 selector.GetOneOption()
71 choice, spicedeck = selector
72 if choice == 10 # 1st run
73     return
74 elsif not [1, 2, 3, 4].inclu
75     puts "! Your choice '#{cho
76     return
77 end
78 AboutCurrentDesign(spicedeck
79
80
81 # Global
82 connect_global
83 connect_global
84
85 # Store the LVS report to th
86 report_lvs( "inv-choice#{choice}.lv
87
88 # Write the extracted netlist to this file
89 target_netlist( "inv-choice#{choice}_extracted.cir",
90               write_spice,
91               "Extracted by KLayout with <#{spicedeck}>" )
92
93 #-----
94 # [3] Drawing layers
95 #-----
96 nwell = input(1, 0)
97 active = input(2, 0)
98 pplus = input(3, 0)
99 nplus = input(4, 0)
100 poly = input(5, 0)
101 contact = input(6, 0)
102 metall = input(7, 0)
103 metall_lbl = labels(7, 1)
104 via1 = input(8, 0)
105 metal2 = input(9, 0)
106 metal2_lbl = labels(9, 1)
107
108 # Bulk layer for terminal provisioning
109 bulk = polygon_layer
110
111 #-----
112 # [4] Computed layers
113 #-----
114
115 active_in_nwell = active & nwell
116 pactive = active in nwell & pplus
117 pgate = pactive & poly
118 psd = pactive - pgate
119
120 active_outside_nwell = active - nwell
121 nactive = active_outside_nwell & nplus
122 ngate = nactive & poly
123 nsd = nactive - ngate
124
125 #-----
126 # [5] Device extraction
127 #-----
128
129 # PMOS transistor device extraction
130 extract_devices(mos4("PMOS"), { "SD" => psd, "G" => pgate, "W" => nwell,
131                                "tS" => psd, "tD" => psd, "tG" => poly, "tW" => nwell })
132
133 # NMOS transistor device extraction
134 extract_devices(mos4("NMOS"), { "SD" => nsd, "G" => ngate, "W" => bulk,
135                                "tS" => nsd, "tD" => nsd, "tG" => poly, "tW" => bulk })
136
137 #-----
138 # [6] Define c
139 #-----
140
141 # Inter-layer
142 connect(psd,
143 connect(nsd,
144 connect(poly,
145 connect(contact,
146 connect(metall,
147 connect(metall,
148 connect(via1,
149 connect(metal2,
150
151 # Global
152 connect_global
153 connect_global
154
155 # Store the LVS report to th
156 report_lvs( "inv-choice#{choice}.lv
157
158 # Write the extracted netlist to this file
159 target_netlist( "inv-choice#{choice}_extracted.cir",
160               write_spice,
161               "Extracted by KLayout with <#{spicedeck}>" )
162
163 # EoF
164
```

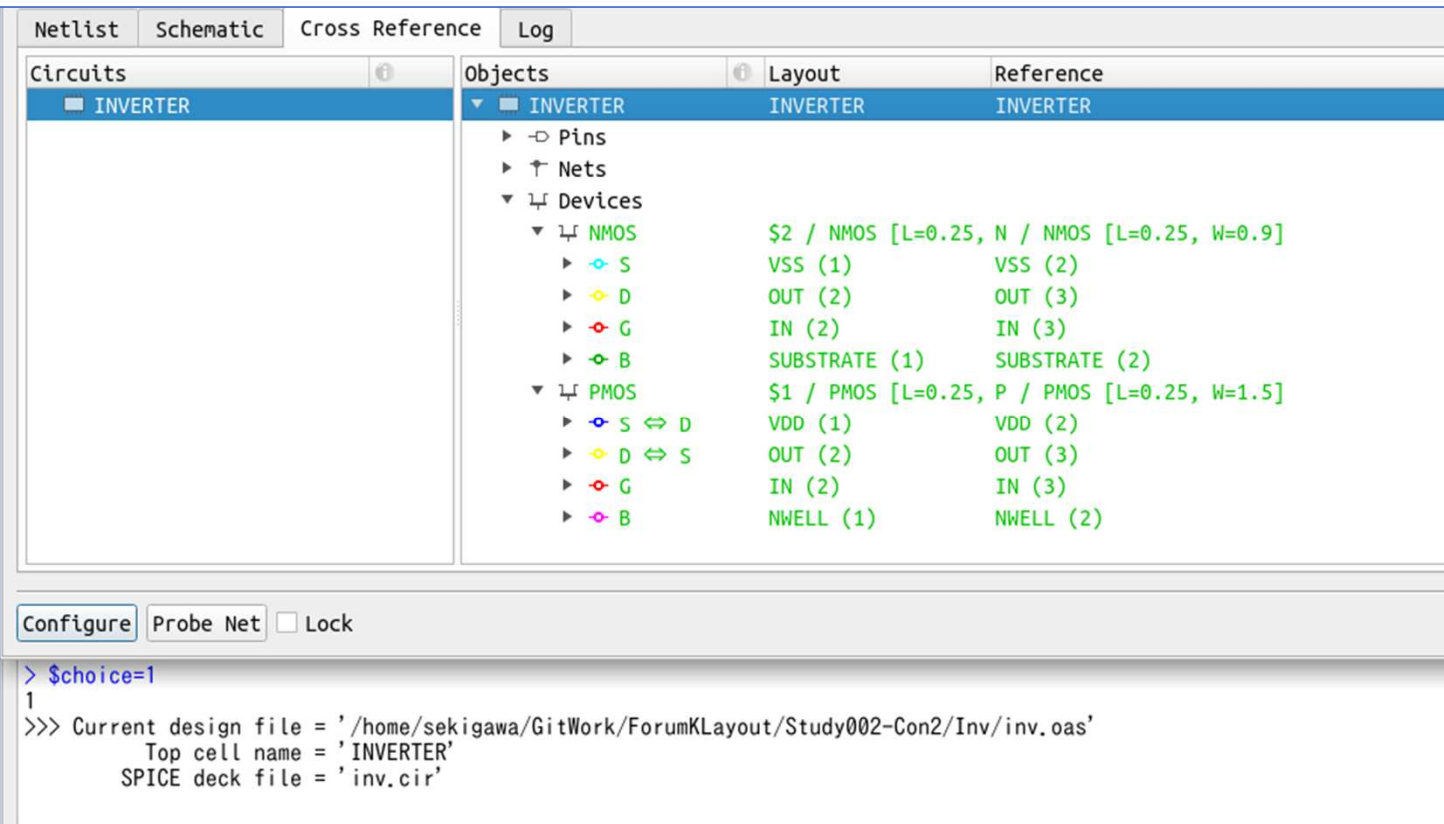
```
1 #
2 # Original: ${klayout_root}/testdata/lvs/inv.lvs
3 #
4 # Modified: inv.lvs
5 # by: Kazzz-S
6 # date: 2023-03-06
7 # aims: 1) retry the four SPICE deck files, namely ["inv.cir", "invX1.cir", "invX2.cir",
8 # "inv-correct.cir"] with the "MOS4" (not "DMOS4") extractor after the issue
9 # in https://github.com/KLayout/klayout/issues/1304 has been fixed
10 #-----
11
12 #-----
13 # [0] Utilities
14 #-----
15
16 def AboutCurrentDesign(spicedeck)
17     designFile = RBA::CellView::active.filename
18     active_layout = RBA::CellView::active.layout
19     puts ">>> Current design file = '#{designFile}'"
20     puts "        Top cell name = '#{active.layout.top_cell.name}'"
21     puts "        SPICE deck file = '#{spicedeck}'"
22 end
23
24 class SpiceDeckSelector
25     def initialize
26         if $choice == nil # global variable to choose a SPICE deck
27             $choice = 10
28         end
29         @spicedeck = [ $choice, "" ]
30
31         @spiceOpt = { 0 => "exit", 1 => "original", 2 => "variantX1", 3 => "variantX2", 4 => "correct" }
32         @spiceDECK = { "original" => "inv.cir", # (PMOS, NMOS)=(incorrect, correct)
33                      "variantX1" => "invX1.cir", # (PMOS, NMOS)=(incorrect, incorrect)
34                      "variantX2" => "invX2.cir", # (PMOS, NMOS)=( correct, incorrect)
35                      "correct" => "inv-correct.cir", # (PMOS, NMOS)=( correct, correct)
36         }
37     end
38
39     def GetSpiceDeck
40         return @spicedeck
41     end
42
43     def GetOneOption
44         case $choice
45         when 0
46             puts "Bye! You can ignore the exception if caught."
47         end
48     end
49 end
```

inv.lvs

21. Using MOS4 for the **inv.cir** Tutorial

4. Run the modified LVS script four times: #1/4

```
1 |  
2 * Simple CMOS inverter circuit : original: (PMOS, NMOS)=(incorrect, correct)  
3  
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD  
5 Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U  
6 Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U  
7 .ENDS  
8
```



21. Using MOS4 for the [inv.cir](#) Tutorial

4. Run the modified LVS script four times: #2/4

```
inv.cir x invX1.cir x invX2.cir x inv-correct.cir x
1
2 * Simple CMOS inverter circuit Variant X1: (PMOS, NMOS)=(incorrect, incorrect)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD $choice=2
5 Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
6 Mn VSS IN OUT SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
9 This net matched as expected.
```

Netlist Schematic Cross Reference Log

Circuits

Objects

Layout

Reference

INVERTER

INVERTER

INVERTER

INVERTER

Pins

Nets

Devices

NMOS

\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]

S ↔ D VSS (1) VSS (2)

D ↔ S OUT (2) OUT (3)

G IN (2) IN (3)

B SUBSTRATE (1) SUBSTRATE (2)

PMOS

\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]

S ↔ D VDD (1) VDD (2)

D ↔ S OUT (2) OUT (3)

G IN (2) IN (3)

B NWELL (1) NWELL (2)

Configure Probe Net Lock

> \$choice=2

2

>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002-Con2/Inv/inv.oas'

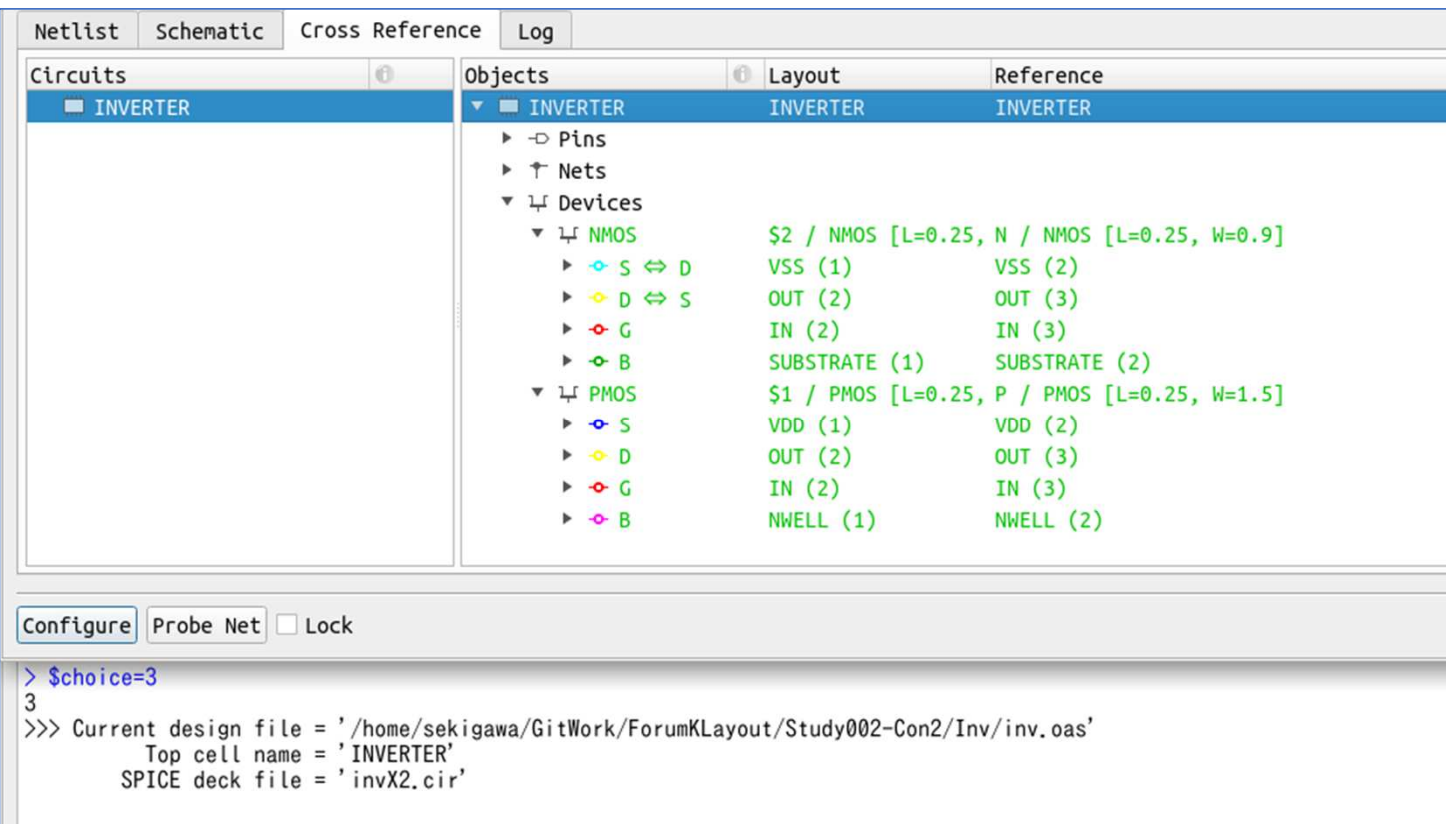
Top cell name = 'INVERTER'

SPICE deck file = 'invX1.cir'

21. Using MOS4 for the **inv.cir** Tutorial

4. Run the modified LVS script four times: #3/4

```
inv.cir x invX1.cir x invX2.cir x inv-correct.cir x
1 |
2 * Simple CMOS inverter circuit Variant X2: (PMOS, NMOS)=( correct, incorrect)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD $choice=3
5 Mp OUT IN VDD NWELL PMOS W=1.5U L=0.25U
6 Mn VSS IN OUT SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
9
```



21. Using MOS4 for the [inv.cir](#) Tutorial

4. Run the modified LVS script four times: #4/4

```
inv.cir x invX1.cir x invX2.cir x inv-correct.cir x
1
2 * Simple CMOS inverter circuit
3 *
4 * Original: ${klayout_root}/testdata/lvs/inv.cir
5 *
6 * Modified: inv-correct.cir PMOS, NMOS)=( correct, correct)
7 * by: Kazzz-S
8 * date: 2023-03-06
9 * aims: 1) correct D-S connections of the PMOS (flipped in the original)
10
11 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
12 * Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
13 Mp OUT IN VDD NWELL PMOS W=1.5U L=0.25U
14 Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U
15 .ENDS
16
```

\$choice=4

This net matched as expected.

Netlist Schematic Cross Reference Log

Circuits

Objects

Layout

Reference

INVERTER

INVERTER

INVERTER

INVERTER

Pins

Nets

Devices

NMOS

\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]

S

VSS (1)

VSS (2)

D

OUT (2)

OUT (3)

G

IN (2)

IN (3)

B

SUBSTRATE (1)

SUBSTRATE (2)

PMOS

\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]

S

VDD (1)

VDD (2)

D

OUT (2)

OUT (3)

G

IN (2)

IN (3)

B

NWELL (1)

NWELL (2)

Configure Probe Net Lock

> \$choice=4

4

>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002-Con2/Inv/inv.oas'

Top cell name = 'INVERTER'

SPICE deck file = 'inv-correct.cir'

KLayout Forum No. 2238 (as Study002: LVS of CMOS Inverter and 2-input NAND)

13

21. Using MOS4 for the [inv.cir](#) Tutorial



NetlistSchematicCross ReferenceLog

Circuits

INVERTER

Objects

INVERTER

Pins

Nets

Devices

NMOS

S

D

G

B

PMOS

S ⇔ D

D ⇔ S

G

B

Layout

INVERTER

\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]

VSS (1)

OUT (2)

IN (2)

SUBSTRATE (1)

\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]

VDD (1)

OUT (2)

IN (2)

NWELL (1)

Reference

INVERTER

VSS (2)

OUT (3)

IN (3)

SUBSTRATE (2)

VDD (2)

OUT (3)

IN (3)

NWELL (2)

Configure

Probe Net

☐ Lock

Only in PMOS, S ⇔ D swapping happened.

> \$choice=1

1

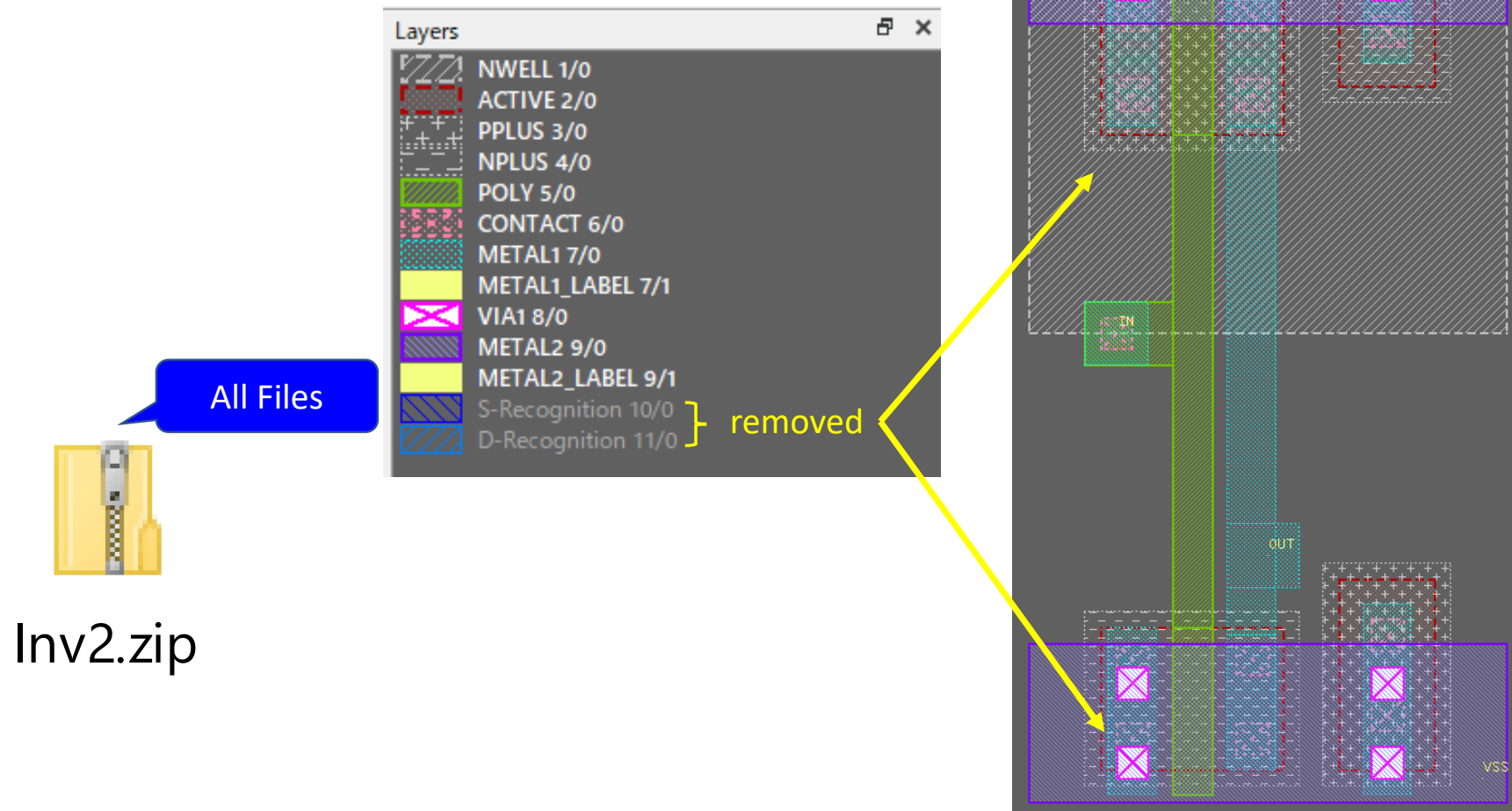
>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002-Con2/Inv/inv.oas'

Top cell name = 'INVERTER'

SPICE deck file = 'inv.cir'

22. Using MOS4 for the **inv2.cir** Tutorial

1. Remove the two dummy layers for S- and D-recognition that were added to use the DMOS4 extractor.



22. Using MOS4 for the `inv2.cir` Tutorial

2. Prepare four SPICE deck files to test all S and D combinations.

```
1
2 * Simple CMOS inverer circuit : original: (PMOS, NMOS)=(incorrect, correct)
3
4 .SUBCKT INVERTER WITH DIODES VSS IN OUT VDD
5 Mp VDD IN OUT VDD PMOS W=1.5U L=0.25U
6 Mn OUT IN VSS VSS NMOS W=0.9U L=0.25U
7 .ENDS
8
```

`$choice=1`

D and S are swapped

```
1
2 * Simple CMOS inverer circuit Variant X1: (PMOS, NMOS)=(incorrect, incorrect)
3
4 .SUBCKT INVERTER WITH DIODES VSS IN OUT VDD
5 Mp VDD IN OUT VDD PMOS W=1.5U L=0.25U
6 Mn VSS IN OUT VSS NMOS W=0.9U L=0.25U
7 .ENDS
8
```

`$choice=2`

```
1
2 * Simple CMOS inverer circuit Variant X2: (PMOS, NMOS)=( correct, incorrect)
3
4 .SUBCKT INVERTER WITH DIODES VSS IN OUT VDD
5 Mp OUT IN VDD VDD PMOS W=1.5U L=0.25U
6 Mn VSS IN OUT VSS NMOS W=0.9U L=0.25U
7 .ENDS
8
```

`$choice=3`

```
1
2 * Simple CMOS inverter circuit
3 *
4 * Original: ${klayout_root}/testdata/lvs/inv2.cir
5 *
6 * Modified: inv2-correct.cir (PMOS, NMOS)=( correct, correct)
7 *   by: Kazzz-S
8 *   date: 2023-03-06
9 *   aims: 1) correct D-S connections of the PMOS (flipped in the original)
10
11 .SUBCKT INVERTER WITH DIODES VSS IN OUT VDD
12 * Mp VDD IN OUT VDD PMOS W=1.5U L=0.25U
13 Mp OUT IN VDD VDD PMOS W=1.5U L=0.25U
14 Mn OUT IN VSS VSS NMOS W=0.9U L=0.25U
15 .ENDS
16
```

`$choice=4`

I expect all four should match by S-D swapping.

22. Using MOS4 for the **inv2.cir** Tutorial

3. Modify the sample LVS script for testing and debugging.

```
1 #-----
2 # Original: ${klayout_root}/testdata/lvs/inv2.lvs
3 #
4 # Modified: inv2.lvs
5 # by: Kazzz-S
6 # date: 2023-03-06
7 # aims: 1) retry the four SPICE deck files, namely ["inv.cir", "invX1.cir", "invX2.cir",
8 #         "inv-correct.cir"] with the "MOS4" (not "DMOS4") extractor after the issue
9 #         in https://github.com/KLayout/klayout/issues/1304 has been fixed
10 #-----
11
12 #-----
13 # [0] Utilities
14 #-----
15 def AboutCurrentDesign(spicedeck)
16     designFile = RBA::CellView::active.filename
17     active_layout = RBA::CellView::active.layout
18     puts ">>> Current design file = '#{designFile}'"
19     puts "        Top cell name = '#{active_layout.top_cell.name}'"
20     puts "        SPICE deck file = '#{spicedeck}'"
21 end
22
23 class SpiceDeckSelector
24     def initialize
25         if $choice == nil # global variable to choose a SPICE deck
26             $choice = 10
27         end
28         @spicedeck = [ $choice, "" ]
29
30         @spiceOpt = { 0 => "exit", 1 => "original", 2 => "variantX1", 3 => "variantX2", 4 => "correct" }
31         @spiceDECK = { "original" => "inv2.cir", # (PMOS, NMOS)=(incorrect, correct)
32                       "variantX1" => "inv2X1.cir", # (PMOS, NMOS)=(incorrect, incorrect)
33                       "variantX2" => "inv2X2.cir", # (PMOS, NMOS)=( correct, incorrect)
34                       "correct" => "inv2-correct.cir", # (PMOS, NMOS)=( correct, correct)
35                     }
36     end
37
38     def GetSpiceDeck
39         return @spicedeck
40     end
41
42     def GetOneOption
43         case $choice
44         when 0
45             puts "Bye! You can ignore the exception if caught."
46         end
47     end
48 end
49
50 #-----
51 # [1] Design
52 #-----
53 dirName, baseName = File.split( RBA::CellView::active.layout.dir, RBA::CellView::active.layout.name )
54 Dir.chdir(dirName)
55
56 source( "inv2.oas", "INVERTER_WITH_DIODES" )
57
58 deep
59
60 selector = SpiceDeckSelector.new
61 selector.GetOneOption()
62 choice, spicedeck = selector.GetSpiceDeck()
63
64 if choice == 10 # 1st run
65     return
66 else
67     puts "! Your choice '#{choice}' is not in [1, 2, 3, 4]. Please try again."
68     return
69 end
70
71 AboutCurrentDesign(spicedeck)
72
73 #-----
74 # [2] Reports
75 #-----
76 # Store the LVS report to this file
77 report_lvs( "inv2-choice#{choice}.lvsdb", true )
78
79 # Write the extracted netlist to this file
80 target_netlist( "inv2-choice#{choice}_extracted.cir",
81                 write_spice,
82                 "Extracted by KLayout with <#{spicedeck}>" )
83
84 #-----
85 # [3] Drawing layers
86 #-----
87 nwell = input(1, 0)
88 active = input(2, 0)
89 pplus = input(3, 0)
90 nplus = input(4, 0)
91 poly = input(5, 0)
92 contact = input(6, 0)
93 metall = input(7, 0)
94 metall_lbl = labels(7, 1)
95 vial = input(8, 0)
96 metall2 = input(9, 0)
97 metall2_lbl = labels(9, 1)
98
99 # Bulk layer for terminal provisioning
100 bulk = polygon_layer
101
102 #-----
103 # [4] Computed layers
104 #-----
105 # Inter-layer
106 connect(psd, d115 active_in_nwell = active & nwell
107 connect(nsd, d116 pactive = active_in_nwell
108 connect(poly, d117 pgate = pactive & poly
109 connect(ntie, d118 psd = pactive - pgate
110 connect(nwell, r119 ntie = active_in_nwell
111 connect(ptie, d120
112 connect(contact, r121 active_outside_nwell = active - nwell
113 connect(metall1, r122 nactive = active_outside_nwell
114 connect(metall1, v123 ngate = nactive & poly
115 connect(vial, r124 nsd = nactive - ngate
116 connect(metall2, r125 ptie = active_outside_nwell
117
118 # Global
119 connect_global(bulk,
120 connect_global(ptie,
121
122 # [5] Device extraction
123 #-----
124 # PMOS transistor device extraction
125 extract_devices(mos4("PMOS"), { "SD" => psd, "G" => pgate, "W" => nwell,
126 # [7] Compare section
127 #-----
128 # NMOS transistor device extraction
129 schematic(spicedeck)
130
131 compare
132
133 # EOF
134
```

inv2.lvs

22. Using MOS4 for the [inv2.cir](#) Tutorial

4. Run the modified LVS script four times: #1/4

```
inv2.cir x inv2X1.cir x inv2X2.cir x inv2-correct.cir x
1 |
2 * Simple CMOS inverter circuit : original: (PMOS, NMOS)=(incorrect, correct)
3
4 .SUBCKT INVERTER WITH DIODES VSS IN OUT VDD
5 Mp VDD IN OUT VDD PMOS W=1.5U L=0.25U
6 Mn OUT IN VSS VSS NMOS W=0.9U L=0.25U
7 .ENDS
8
```

\$choice=1

This net matched as expected.

Netlist Schematic Cross Reference Log

Circuits

INVERTER_WITH_DIODES

Objects

Layout

Reference

INVERTER_WITH_DIODES

Pins

Nets

Devices

NMOS

\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]

S

VSS (2)

VSS (3)

D

OUT (2)

OUT (3)

G

IN (2)

IN (3)

B

VSS (2)

VSS (3)

PMOS

\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]

S ↔ D

VDD (2)

VDD (3)

D ↔ S

OUT (2)

OUT (3)

G

IN (2)

IN (3)

B

VDD (2)

VDD (3)

Configure

Probe Net

☐ Lock

> \$choice=1

1

>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002-Con2/Inv2/inv2.oas'

Top cell name = 'INVERTER_WITH_DIODES'

SPICE deck file = 'inv2.cir'

22. Using MOS4 for the [inv2.cir](#) Tutorial

4. Run the modified LVS script four times: #2/4

```
inv2.cir x inv2X1.cir x inv2X2.cir x inv2-correct.cir x
1
2 * Simple CMOS inverter circuit Variant X1: (PMOS, NMOS)=(incorrect, incorrect)
3
4 .SUBCKT INVERTER WITH DIODES VSS IN OUT VDD $choice=2
5 Mp VDD IN OUT VDD PMOS W=1.5U L=0.25U
6 Mn VSS IN OUT VSS NMOS W=0.9U L=0.25U
7 .ENDS
8
9 This net matched as expected.
```

Netlist Schematic Cross Reference Log

Circuits

INVERTER_WITH_DIODES

Objects

Layout

Reference

INVERTER_WITH_DIODES

Pins

Nets

Devices

NMOS

\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]

S ↔ D

VSS (2)

VSS (3)

D ↔ S

OUT (2)

OUT (3)

G

IN (2)

IN (3)

B

VSS (2)

VSS (3)

PMOS

\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]

S ↔ D

VDD (2)

VDD (3)

D ↔ S

OUT (2)

OUT (3)

G

IN (2)

IN (3)

B

VDD (2)

VDD (3)

Configure

Probe Net

☐ Lock

> \$choice=2

2

>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002-Con2/Inv2/inv2.oas'

Top cell name = 'INVERTER_WITH_DIODES'

SPICE deck file = 'inv2X1.cir'

22. Using MOS4 for the [inv2.cir](#) Tutorial

4. Run the modified LVS script four times: #3/4

```
1  
2 * Simple CMOS inverter circuit Variant X2: (PMOS, NMOS)=( correct, incorrect  
3  
4 .SUBCKT INVERTER WITH DIODES VSS IN OUT VDD  
5 Mp OUT IN VDD VDD PMOS W=1.5U L=0.25U $choice=3  
6 Mn VSS IN OUT VSS NMOS W=0.9U L=0.25U  
7 .ENDS  
8 | This net matched as expected.
```

The screenshot displays the KiCad EDA software interface, specifically the 'Cross Reference' panel. The top tabs include 'Netlist', 'Schematic', 'Cross Reference', and 'Log'. The 'Cross Reference' panel is active, showing a table with columns: 'Circuits', 'Objects', 'Layout', and 'Reference'.

The 'Circuits' column shows the selected circuit: 'INVERTER_WITH_DIODES'. The 'Objects' column lists the components and their properties:

- Pins**
- Nets**
- Devices**
 - NMOS**
 - S ↔ D
 - D ↔ S
 - G
 - B
 - PMOS**
 - S
 - D
 - G
 - B

The 'Layout' column shows the component names and their properties, and the 'Reference' column shows the reference designators. The table is as follows:

Circuits	Objects	Layout	Reference
INVERTER_WITH_DIODES	INVERTER_WITH_DIODES	INVERTER_WITH_DIODES	INVERTER_WITH_DIODES
	Pins		
	Nets		
	Devices		
	NMOS	\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]	
	S ↔ D	VSS (2)	VSS (3)
	D ↔ S	OUT (2)	OUT (3)
	G	IN (2)	IN (3)
	B	VSS (2)	VSS (3)
	PMOS	\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]	
	S	VDD (2)	VDD (3)
	D	OUT (2)	OUT (3)
	G	IN (2)	IN (3)
	B	VDD (2)	VDD (3)

At the bottom of the interface, there is a 'Configure' button, a 'Probe Net' checkbox, and a 'Lock' checkbox. Below these, a command prompt shows the following commands and their output:

```
> $choice=3
3
>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002-Con2/Inv2/inv2.oas'
      Top cell name = 'INVERTER_WITH_DIODES'
      SPICE deck file = 'inv2X2.cir'
```

22. Using MOS4 for the inv2.cir Tutorial

4. Run the modified LVS script four times: #4/4

NetlistSchematicCross ReferenceLog

Circuits

INVERTER_WITH_DIODES

Objects

INVERTER_WITH_DIODES

Pins

Nets

Devices

NMOS

\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]

S

VSS (2)

VSS (3)

D

OUT (2)

OUT (3)

G

IN (2)

IN (3)

B

VSS (2)

VSS (3)

PMOS

\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]

S

VDD (2)

VDD (3)

D

OUT (2)

OUT (3)

G

IN (2)

IN (3)

B

VDD (2)

VDD (3)

Configure

Probe Net

☐ Lock

> \$choice=4

4

>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002-Con2/Inv2/inv2.oas'

Top cell name = 'INVERTER_WITH_DIODES'

SPICE deck file = 'inv2-correct.cir'

inv2.cirxinv2X1.cirxinv2X2.cirxinv2-correct.cirx

```
1
2 * Simple CMOS inverter circuit
3 *
4 * Original: ${klayout_root}/testdata/lvs/inv2.cir
5 *
6 * Modified: inv2-correct.cir (PMOS, NMOS)=( correct, correct)
7 *   by: Kazzz-S
8 *   date: 2023-03-06
9 *   aims: 1) correct D-S connections of the PMOS (flipped in the original)
10
11 .SUBCKT INVERTER WITH DIODES VSS IN OUT VDD
12 * Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
13 Mp OUT IN VDD VDD PMOS W=1.5U L=0.25U
14 Mn OUT IN VSS VSS NMOS W=0.9U L=0.25U
15 .ENDS
16
```

This net matched as expected.

22. Using MOS4 for the [inv2.cir](#) Tutorial



NetlistSchematicCross ReferenceLog

Circuits

INVERTER_WITH_DIODES

Objects

INVERTER_WITH_DIODES

Pins

Nets

Devices

NMOS

S

D

G

B

PMOS

S ↔ D

D ↔ S

G

B

Layout

INVERTER_WITH_DIODES

Reference

INVERTER_WITH_DIODES

Configure

Probe Net

☐ Lock

Only in PMOS, S ↔ D swapping happened.

> \$choice=1

1

>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002-Con2/Inv2/inv2.oas'

Top cell name = 'INVERTER_WITH_DIODES'

SPICE deck file = 'inv2.cir'

KLayout Forum No. 2238 (as Study002: LVS of CMOS Inverter and 2-input NAND)

22

23. Using MOS4 for a 2-input NAND



WENSHIH

February 17

https://www.klayout.de/forum/discussion/comment/_9493

on 2023-02-17

Thanks for your suggestion and helps! If there is any information I can supply, please tell me.
Here is the test file.

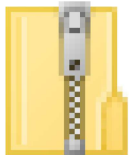


nand.test.zip
14.7K



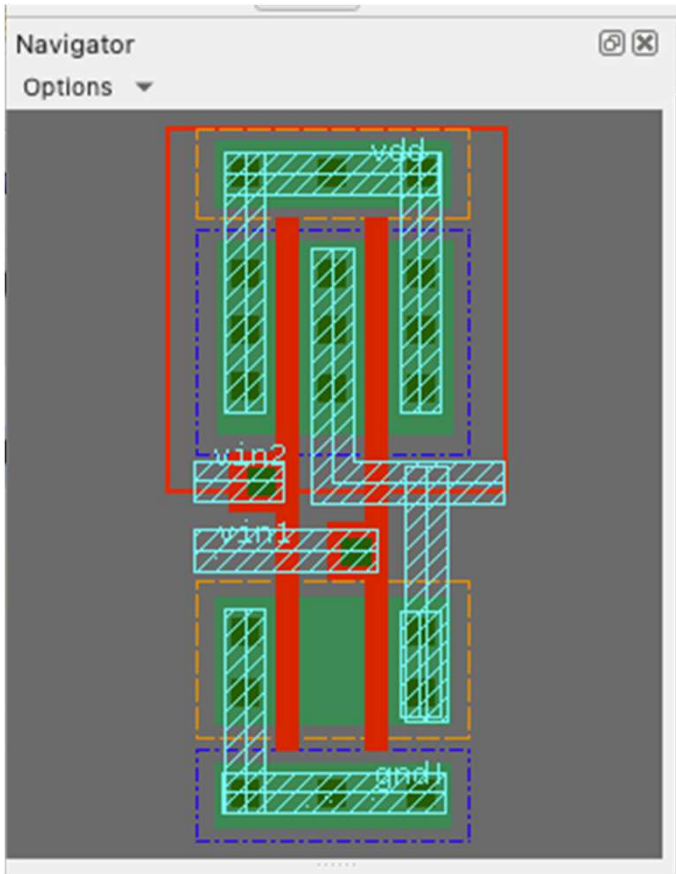
Starting point. Thank you for providing this!

1. Check the provided resource files and modify them if necessary.



All Files

NAND.zip



23. Using MOS4 for a 2-input NAND

Cells

▼ nand

▶ M1_M5

▶ M1_M5\$1

▶ M1_M6

▶ M1_M6\$1

M1_V1_M2

M1_V1_M2\$1

M5_V5_M6

M5_V5_M6\$1

NCELL\$\$\$33500204

NCELL\$\$\$33500204\$1

NCELL\$\$\$33501228

NCELL\$\$\$33501228\$1

NCELL\$\$\$33504300

NCELL\$\$\$33504300\$1

PCELL\$\$\$33495084

PCELL\$\$\$33495084\$1

PCELL\$\$\$33496108

PCELL\$\$\$33496108\$1

PCELL\$\$\$33497132

PCELL\$\$\$33497132\$1

PCELL\$\$\$33498156

PCELL\$\$\$33498156\$1

PO_CO_M1

PO_CO_M1\$1

nimp_vdd_noCO

nimp_vdd_noCO\$1

npimp

npimp\$1

pimp_gnd_noCO

pimp_gnd_noCO\$1

Too many ghost cells

Levels 0 .. 3



Cells

▼ nand

▶ M1_M5

▶ M1_M5\$1

▶ M1_M6

▶ M1_M6\$1

M1_V1_M2

M1_V1_M2\$1

M5_V5_M6

M5_V5_M6\$1

NCELL\$\$\$33500204

NCELL\$\$\$33500204\$1

NCELL\$\$\$33501228

NCELL\$\$\$33501228\$1

NCELL\$\$\$33504300

NCELL\$\$\$33504300\$1

PCELL\$\$\$33495084

PCELL\$\$\$33495084\$1

PCELL\$\$\$33496108

PCELL\$\$\$33496108\$1

PCELL\$\$\$33497132

PCELL\$\$\$33497132\$1

PCELL\$\$\$33498156

PCELL\$\$\$33498156\$1

PO_CO_M1

PO_CO_M1\$1

nimp_vdd_noCO

nimp_vdd_noCO\$1

npimp

npimp\$1

pimp_gnd_noCO

pimp_gnd_noCO\$1

Levels 0 .. 1



I need only the top cell.

Navigator

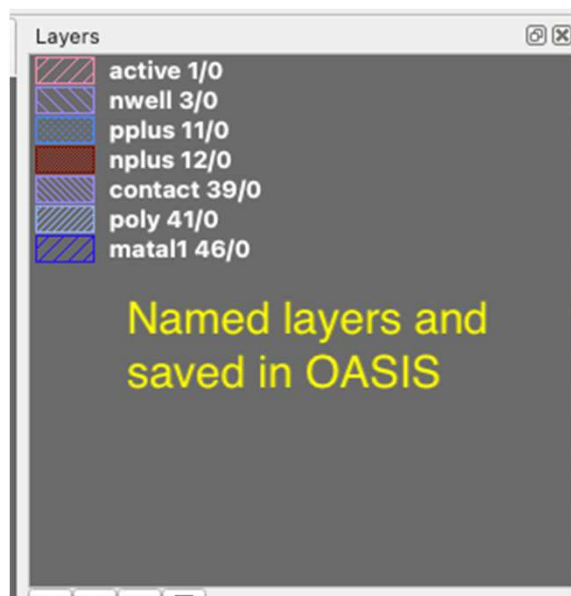
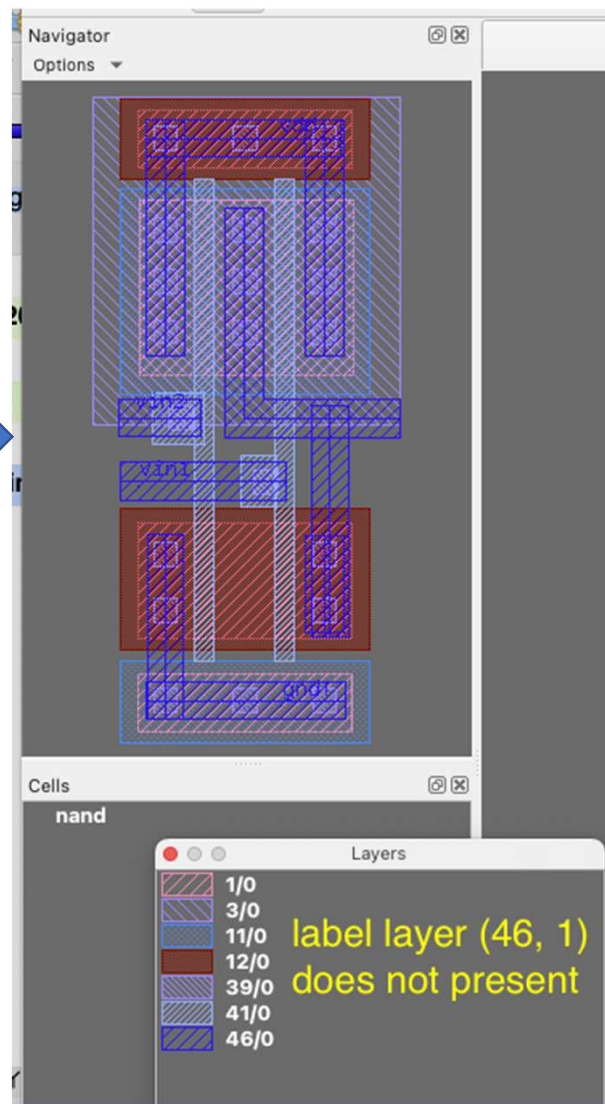
Options ▼

Cells

nand

23. Using MOS4 for a 2-input NAND

```
11 # Drawing layers:
12
13 poly = input(41, 0)
14 active = input(1, 0)
15 nwell = input(3, 0)
16 gate = poly & active
17 nplus = input(12, 0)
18 pplus = input(11, 0)
19 #nplus_od = nplus & active
20 #pplus_od = pplus & active
21 #nplus_od_nw = nplus & active & nwell
22 #pplus_od_nw = pplus & active & nwell
23 contact = input(39, 0)
24 metal1 = input(46, 0)
25 metal1_lbl = labels(46, 1)
26 via1 = input(47, 0)
27 metal2 = input(48, 0)
28 metal2_lbl = labels(48, 1)
29 via2 = input(49, 0)
30 metal3 = input(50, 0)
31 metal3_lbl = labels(50, 1)
32 # Bulk layer for terminal provisioning
33
```



23. Using MOS4 for a 2-input NAND

2. Using `nandSpice16.py`, prepare 16 distinct SPICE deck files that cover all D-S permutations/combinations.

```
nand-choice01.cir x nand-choice08.cir x nand-choice16.cir x
1 |* KLayout Forum: https://www.klayout.de/forum/discussion/2238/
2 |*
3 |* SPICE deck file for WENSHIH's 2-input NAND
4 |* generator = <nandSpice16.py> by Kazzz-S
5 |* choice = 1
6 |* status = [original] all D-S pairs are connected correctly
7 |*
8 |.SUBCKT nand VDD GND
9 |M M6 GND VIN2 N15943 SUBSTRATE NMOS L=0.18um W=1.08um
10 |M M3 N15943 VIN1 OUT SUBSTRATE NMOS L=0.18um W=1.08um
11 |M M5 VDD VIN1 OUT NWELL PMOS L=0.18um W=1.62um
12 |M M4 VDD VIN2 OUT NWELL PMOS L=0.18um W=1.62um
13 |.ENDS

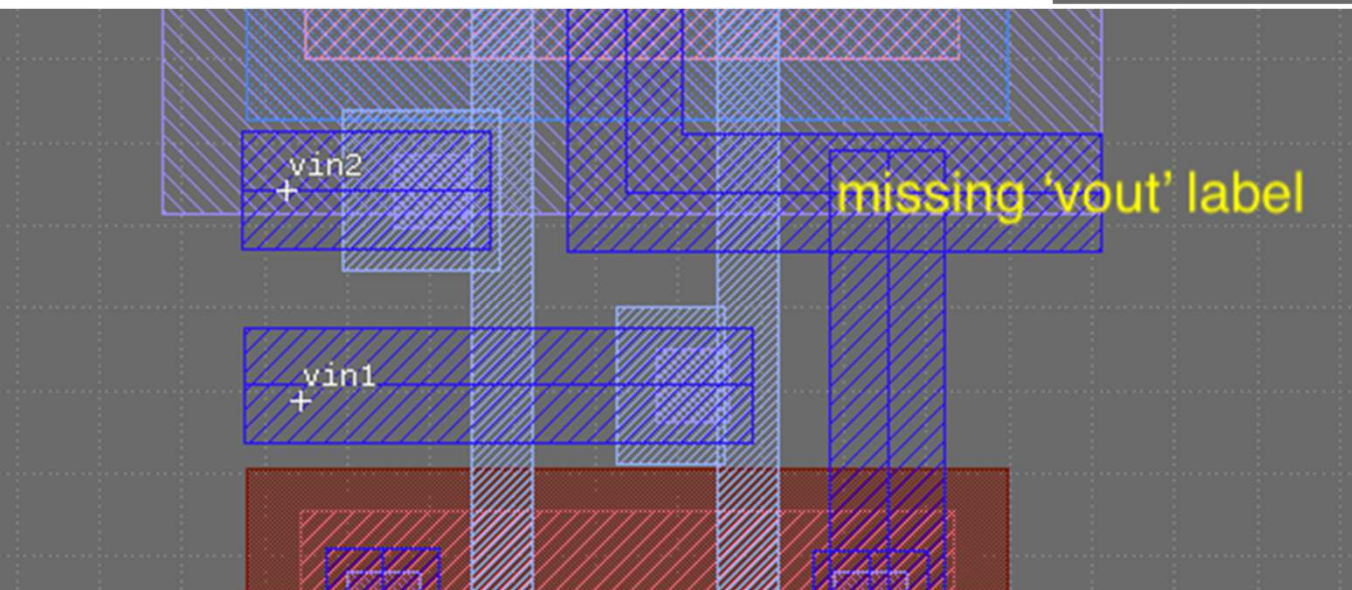
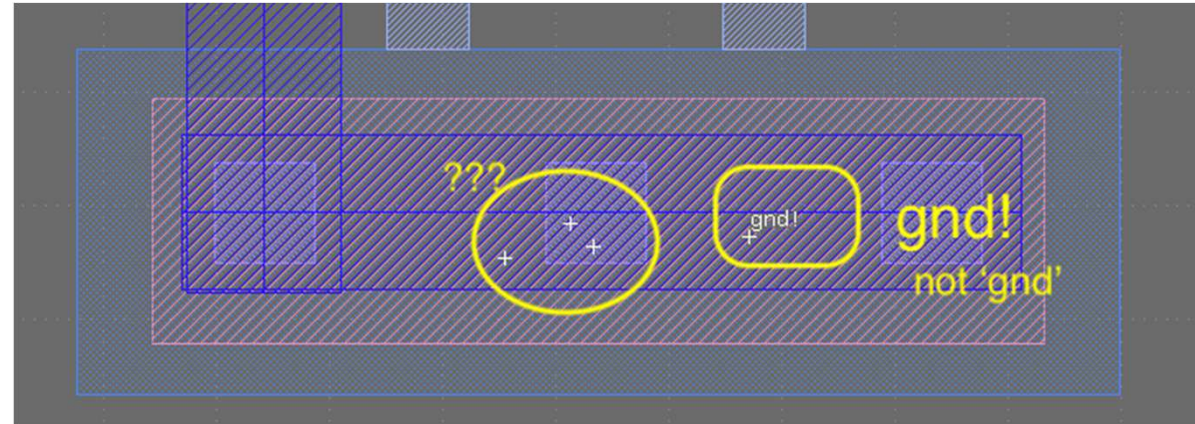
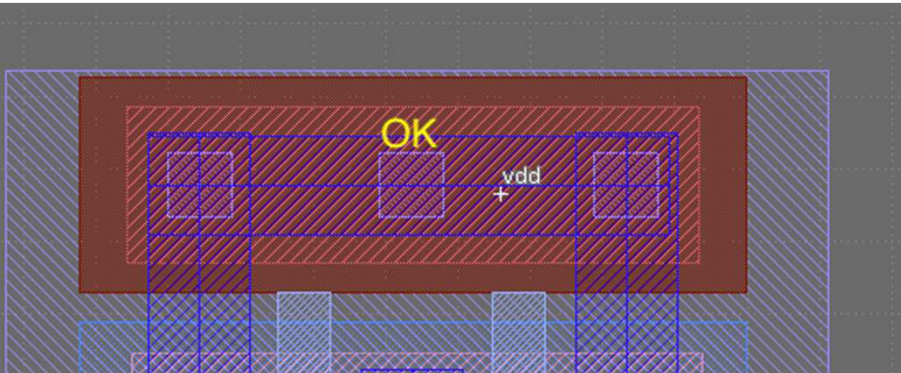
nand-choice01.cir x nand-choice08.cir x nand-choice16.cir x
1 |* KLayout Forum: https://www.klayout.de/forum/discussion/2238/
2 |*
3 |* SPICE deck file for WENSHIH's 2-input NAND
4 |* generator = <nandSpice16.py> by Kazzz-S
5 |* choice = 8
6 |* status = [incorrect] at least one D-S pair is swapped
7 |*
8 |.SUBCKT nand VDD GND IN1 IN2 OUT NWELL SUBSTRATE
9 |M M6 N15943 VIN2 GND SUBSTRATE NMOS L=0.18um W=1.08um
10 |M M3 OUT VIN1 N15943 SUBSTRATE NMOS L=0.18um W=1.08um
11 |M M5 OUT VIN1 VDD NWELL PMOS L=0.18um W=1.62um
12 |M M4 OUT VIN2 VDD NWELL PMOS L=0.18um W=1.62um
13 |.ENDS

nand-choice01.cir x nand-choice08.cir x nand-choice16.cir x
1 |* KLayout Forum: https://www.klayout.de/forum/discussion/2238/
2 |*
3 |* SPICE deck file for WENSHIH's 2-input NAND
4 |* generator = <nandSpice16.py> by Kazzz-S
5 |* choice = 16
6 |* status = [correct] all D-S pairs are connected correctly
7 |*
8 |.SUBCKT nand VDD GND IN1 IN2 OUT NWELL SUBSTRATE
9 |M M6 N15943 VIN2 GND SUBSTRATE NMOS L=0.18um W=1.08um
10 |M M3 OUT VIN1 N15943 SUBSTRATE NMOS L=0.18um W=1.08um
11 |M M5 OUT VIN1 VDD NWELL PMOS L=0.18um W=1.62um
12 |M M4 OUT VIN2 VDD NWELL PMOS L=0.18um W=1.62um
13 |.ENDS
```

I expect ALL 16 SPICE deck files should match by S-D swapping.

23. Using MOS4 for a **2-input NAND**

3. Check the original design in GDS2.



23. Using MOS4 for a 2-input NAND

- 4. Remove the four dummy layers for S- and D-recognition that were added to use the DMOS4 extractor.

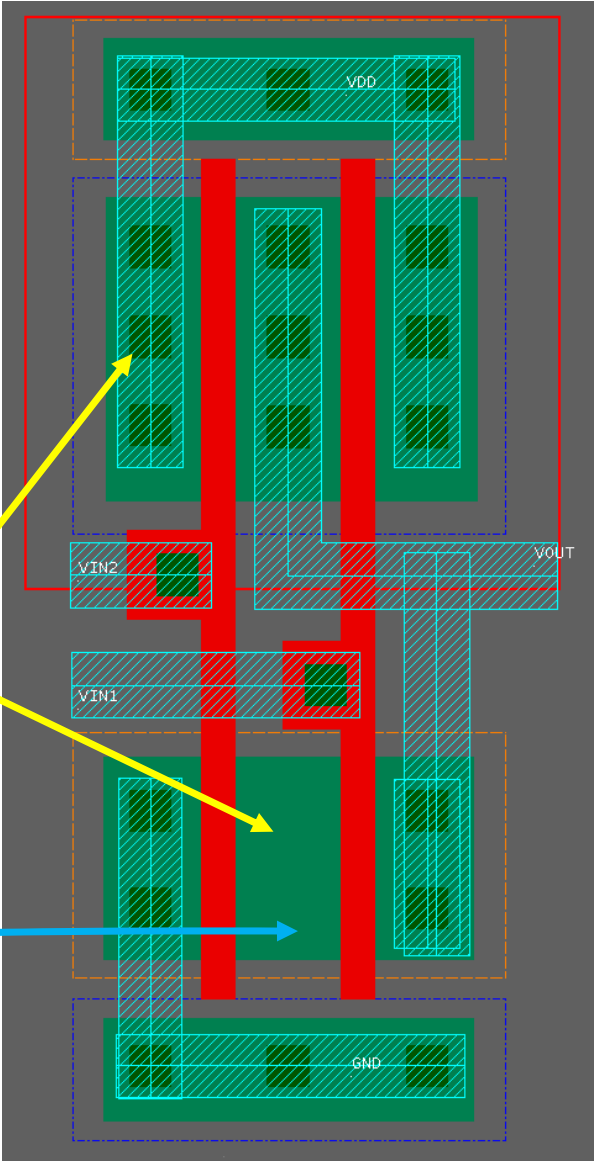
Monoecy ([/məˈniːsi/](#); adj. **monoecious** [/məˈniːʃəs/](#)^[1] is a [sexual system](#) in [seed plants](#) where separate [male](#) and [female](#) cones or flowers are present on the same plant.

[Monoecy - Wikipedia](#)

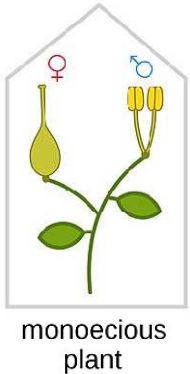
Layers

	active 1/0
	nwell 3/0
	pplus 11/0
	nplus 12/0
	poly 41/0
	contact 39/0
	metal1 46/0
	metal1_lbs 46/1
	S-Recognition 51/0
	MaleS-Recognition 51/1
	D-Recognition 52/0
	FemaleD-Recognition 52/1

} removed



No geometrical hint implying *monoecy* is given.



23. Using MOS4 for a 2-input NAND

5. Modify the LVS script for testing and debugging.

```
91 report_lvs( "nand-choice%02d.lvsdb"
92
93 # Write the extracted netlist to th
94 target_netlist( "nand-choice%02d_e
95               write_spice,
96               "Extracted by KLayout
97
98 #-----
99 # [3] Drawing layers
100 #-----
101 active      = input(1, 0)
102 nwell       = input(3, 0)
103 pplus      = input(11, 0)
104 nplus      = input(12, 0)
105 poly       = input(41, 0)
106 contact    = input(39, 0)
107 metall     = input(46, 0)
108 metall_lbl = labels(46, 1)
109
110 # Bulk layer for terminal provision
111 bulk = polygon_layer
112
113 # [6] Defin
114 #-----
115 # Inter-lay
116 # [4] Computed layers
117 #-----
118 active_in_nwell = active & nwell
119 pactive         = active & nplus
120 pgate          = pactive & pplus
121 psd            = pactive & pplus
122 #ntie          = active_in_n
123
124 active_outside_nwell = active - nwell
125 nactive              = active & nplus
126 ngate                = nactive & pplus
127 nsd                  = nactive - n
128 #ptie                = active_out
129
130 # [7] Compa
131 #-----
132 # [5] Device extraction
133 #-----
134 # PMOS transistor device extraction
135 extract_devices(mos4("PMOS"), { "SD" => psd, "G" => pgate, "W" => nwell,
```

```
1 #-----
2 # Original: "lvs 2 1.lvlvs" in the attached ZIP file of
3 # https://www.klayout.de/forum/discussion/comment/9493/#Comment_9493
4 #
5 # Modified: nand-MOS4.lvs
6 # by: Kazzzz-S
7 # date: 2023-03-08
8 # aims: 1) test WENSHIH's NAND circuit with 16 SPICE decks covering all D-S permutations
9 #        2) use the "MOS4" extractor after the issue
10 #        in https://github.com/KLayout/klayout/issues/1304 has been fixed
11 #-----
12
13 #-----
14 # [0] Utilities
15 #-----
16 def AboutCurrentDesign(spicedeck)
17     designFile = RBA::CellView::active.filename
18     activeLayout = RBA::CellView::active.layout
19     puts ">>> Current design file = '#{designFile}'"
20     puts "    Top cell name = '#{activeLayout.top_cell.name}'"
21     puts "    SPICE deck file = '#{spicedeck}'"
22 end
23
24 class SpiceDeckSelector
25     def initialize
26         if $choice == nil # global variable to choose a SPICE deck
27             $choice = 20
28         end
29         @spicedeck = [ $choice, "" ]
30
31         @spiceOpt = {}
32         @spiceOpt[0] = "exit"
33         for choice in Range.new(1, 16) do
34             @spiceOpt[choice] = "choice%02d" % choice
35         end
36
37         @spiceDECK = {}
38         for choice in Range.new(1, 16) do
39             opt = @spiceOpt[choice]
40             @spiceDECK[opt] = "nand-#{opt}.cir"
41         end
42     end
43
44     def GetSpiceDeck
45         return @spicedeck
46     end
47 end
48
49 def GetOneOption
50     case $choice
51     when 0
52         puts "Bye! You can ignore th
53         exit
54     when 1..16
55         @spicedeck = [ $choice, @spic
56     else
57         puts "### Usage [ 0=>exit, k=
58         puts "    Set one of above
59         puts "    then, execute the
60         return
61     end
62 end
63
64 # [1] Design
65 #-----
66 dirName, baseName = File.split( RBA::
67 Dir.chdir(dirName)
68
69 source( "nand.oas", "nand" )
70
71 deep
72
73 selector = SpiceDeckSelector.new
74 selector.GetOneOption()
75 choice, spicedeck = selector.GetSpice
76 if choice == 20 # 1st run
77     return
78 elsif not Range.new(1, 16).include?(c
79     puts "! Your choice '#{choice}' is not in [1..16]"
80     return
81 end
82 AboutCurrentDesign(spicedeck)
83
84 #-----
85 # [2] Reports
86 #-----
87 #-----
88 # Store the LVS report to this file
89 #-----
90
```

nand-MOS4.lvs

6. Run the modified LVS script 16 times.

23. Using MOS4 for a 2-input NAND



Video choice=[1..16]

Still images are in



NAND.zip

NetlistSchematicCross ReferenceLog

Circuits

Objects

Layout

Reference

nand ↔ NAND

nand ↔ NAND

nand

NAND

▶ Pins

▶ Nets

▶ Devices

▶ NMOS

▶ NMOS

▶ PMOS

▶ PMOS

\$3 / NMOS [L=0.18, _M6 / NMOS [L=0.18, W=1.08]

\$4 / NMOS [L=0.18, _M3 / NMOS [L=0.18, W=1.08]

\$2 / PMOS [L=0.18, _M5 / PMOS [L=0.18, W=1.62]

\$1 / PMOS [L=0.18, _M4 / PMOS [L=0.18, W=1.62]

▶ S ↔ D

▶ D ↔ S

▶ G

▶ B

▶ S ↔ D

▶ D ↔ S

▶ G

▶ B

▶ S ↔ D

▶ D ↔ S

▶ G

▶ B

GND (1)

\$7 (2)

VIN2 (2)

SUBSTRATE (2)

\$7 (2)

VOUT (3)

VIN1 (2)

SUBSTRATE (2)

VOUT (3)

VDD (2)

VIN1 (2)

NWELL (2)

VDD (2)

VOUT (3)

VIN2 (2)

NWELL (2)

GND (2)

N15943 (2)

VIN2 (2)

SUBSTRATE (3)

N15943 (2)

OUT (4)

VIN1 (2)

SUBSTRATE (3)

OUT (4)

VDD (3)

VIN1 (2)

NWELL (3)

VDD (3)

OUT (4)

VIN2 (2)

NWELL (3)

Configure

Probe Net

Lock

Only in PMOS _M5, S <=> D swapping did not happen.

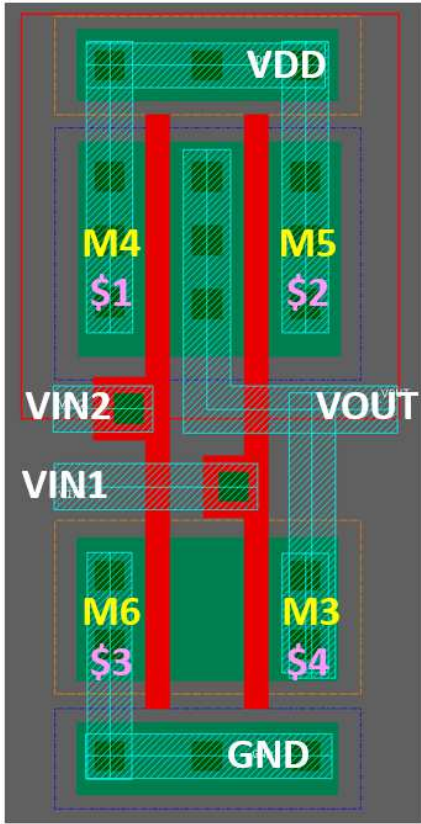
> \$choice=1

1

>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002-Con2/NAND/nand.oas'

Top cell name = 'nand'

SPIICE deck file = 'nand-choice01.cir'



23. Using MOS4 for a 2-input NAND

NetlistSchematicCross ReferenceLog

Circuits

nand ↔ NAND

Objects

nand ↔ NAND

	nand	NAND
↳ Pins		
↳ Nets		
↳ Devices		
↳ NMOS	\$3 / NMOS [L=0.18, _M6 / NMOS [L=0.18, W=1.08]	
↳ S ↔ D	GND (1)	GND (2)
↳ D ↔ S	\$7 (2)	N15943 (2)
↳ G	VIN2 (2)	VIN2 (2)
↳ B	SUBSTRATE (2)	SUBSTRATE (3)
↳ NMOS	\$4 / NMOS [L=0.18, _M3 / NMOS [L=0.18, W=1.08]	
↳ S ↔ D	\$7 (2)	N15943 (2)
↳ D ↔ S	VOUT (3)	OUT (4)
↳ G	VIN1 (2)	VIN1 (2)
↳ B	SUBSTRATE (2)	SUBSTRATE (3)
↳ PMOS	\$2 / PMOS [L=0.18, _M5 / PMOS [L=0.18, W=1.62]	
↳ S	VOUT (3)	OUT (4)
↳ D	VDD (2)	VDD (3)
↳ G	VIN1 (2)	VIN1 (2)
↳ B	NWELL (2)	NWELL (3)
↳ PMOS	\$1 / PMOS [L=0.18, _M4 / PMOS [L=0.18, W=1.62]	
↳ S ↔ D	VDD (2)	VDD (3)
↳ D ↔ S	VOUT (3)	OUT (4)
↳ G	VIN2 (2)	VIN2 (2)
↳ B	NWELL (2)	NWELL (3)

ConfigureProbe NetLock

> \$choice=1
1
>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002-Con2/NAND/nand.oas'
Top cell name = 'nand'
SPICE deck file = 'nand-choice01.cir'

nand-choice01.cirx nand-choice08.cirx nand-choice16.cirx

1 | * KLayout Forum: <https://www.klayout.de/forum/discussion/2238/>
2 *
3 * SPICE deck file for WENSHIH's 2-input NAND
4 * generator = <nandSpice16.py> by Kazzzz-S
5 * choice = 1
6 * status = [original and incorrect] all D-S pairs are completely swapped
7 *
8 .SUBCKT nand VDD GND IN1 IN2 OUT NWELL SUBSTRATE
9 M M6 GND VIN2 N15943 SUBSTRATE NMOS L=0.18um W=1.08um
10 M M3 N15943 VIN1 OUT SUBSTRATE NMOS L=0.18um W=1.08um
11 M M5 VDD VIN1 OUT NWELL PMOS L=0.18um W=1.62um
12 M M4 VDD VIN2 OUT NWELL PMOS L=0.18um W=1.62um
13 .ENDS

WENSHIH's 2-input NAND
<https://www.klayout.de/forum/discussion/2238/>

23. Using MOS4 for a 2-input NAND

NetlistSchematicCross ReferenceLog

Circuits

ObjectsLayoutReference

nand ↔ NAND

VDD

VIN2

VIN1

VOUT

GND

M4 \$1

M5 \$2

M6 \$3

M3 \$4

↪ Pins

↑ Nets

↳ Devices

↳ NMOS

\$3 / NMOS [L=0.18, _M6 / NMOS [L=0.18, W=1.08]

↳ S

GND (1) GND (2)

↳ D

\$7 (2) N15943 (2)

↳ G

VIN2 (2) VIN2 (2)

↳ B

SUBSTRATE (2) SUBSTRATE (3)

↳ NMOS

\$4 / NMOS [L=0.18, _M3 / NMOS [L=0.18, W=1.08]

↳ S

\$7 (2) N15943 (2)

↳ D

VOUT (3) OUT (4)

↳ G

VIN1 (2) VIN1 (2)

↳ B

SUBSTRATE (2) SUBSTRATE (3)

↳ PMOS

\$2 / PMOS [L=0.18, _M5 / PMOS [L=0.18, W=1.62]

↳ S ↔ D

VOUT (3) OUT (4)

↳ D ↔ S

VDD (2) VDD (3)

↳ G

VIN1 (2) VIN1 (2)

↳ B

NWELL (2) NWELL (3)

↳ PMOS

\$1 / PMOS [L=0.18, _M4 / PMOS [L=0.18, W=1.62]

↳ S

VDD (2) VDD (3)

↳ D

VOUT (3) OUT (4)

↳ G

VIN2 (2) VIN2 (2)

↳ B

NWELL (2) NWELL (3)

ConfigureProbe NetLock

> \$choice=16

16

>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002-Con2/NAND/nand.oas'

Top cell name = 'nand'

SPICE deck file = 'nand-choice16.cir'

nand-choice01.cirx nand-choice08.cirx nand-choice16.cirx

1 | * KLayout Forum: <https://www.klayout.de/forum/discussion/2238/>

2 | *

3 | * SPICE deck file for WENSHIH's 2-input NAND

4 | * generator = <nandSpice16.py> by Kazzz-S

5 | * choice = 16

6 | * status = [correct] all D-S pairs are connected correctly

7 | *

8 | .SUBCKT nand VDD GND IN1 IN2 OUT NWELL SUBSTRATE

9 | M M6 N15943 VIN2 GND SUBSTRATE NMOS L=0.18um W=1.08um

10 | M M3 OUT VIN1 N15943 SUBSTRATE NMOS L=0.18um W=1.08um

11 | M M5 OUT VIN1 VDD NWELL PMOS L=0.18um W=1.62um

12 | M M4 OUT VIN2 VDD NWELL PMOS L=0.18um W=1.62um

13 | .ENDS

VDD

WENSHIH's 2-input NAND

<https://www.klayout.de/forum/discussion/2238/>

Vin1

Vin2

Vout

GND

M4

M5

M3

M6

8.1

8.1

5.4

5.4

0.9

0.9

0.9

0.9

23. Using MOS4 for a 2-input NAND



Video choice=[1, 16]

Still images are in



NAND.zip

NetlistSchematicCross ReferenceLog

Circuits

ObjectsLayoutReference

nand ↔ NAND

▼ nand ↔ NAND

nandNAND

► Pins

► Nets

▼ Devices

▼ NMOS

\$3 / NMOS [L=0.18, _M6 / NMOS [L=0.18, W=1.08]

► S ↔ D

GND (1)GND (2)

► D ↔ S

\$7 (2)N15943 (2)

► G

VIN2 (2)VIN2 (2)

► B

SUBSTRATE (2)SUBSTRATE (3)

▼ NMOS

\$4 / NMOS [L=0.18, _M3 / NMOS [L=0.18, W=1.08]

► S ↔ D

\$7 (2)N15943 (2)

► D ↔ S

VOUT (3)OUT (4)

► G

VIN1 (2)VIN1 (2)

► B

SUBSTRATE (2)SUBSTRATE (3)

▼ PMOS

\$2 / PMOS [L=0.18, _M5 / PMOS [L=0.18, W=1.62]

► S

VOUT (3)OUT (4)

► D

VDD (2)VDD (3)

► G

VIN1 (2)VIN1 (2)

► B

NWELL (2)NWELL (3)

▼ PMOS

\$1 / PMOS [L=0.18, _M4 / PMOS [L=0.18, W=1.62]

► S ↔ D

VDD (2)VDD (3)

► D ↔ S

VOUT (3)OUT (4)

► G

VIN2 (2)VIN2 (2)

► B

NWELL (2)NWELL (3)

ConfigureProbe NetLock

Only in PMOS _M5, S <=> D swapping did not happen.

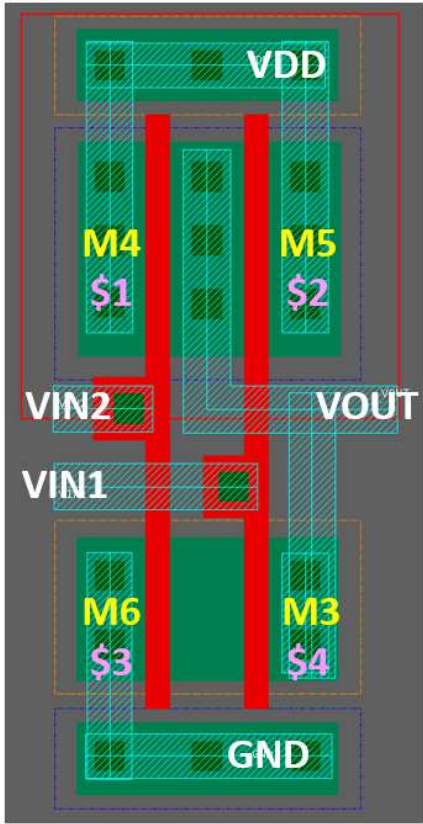
> \$choice=1

1

>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002-Con2/NAND/nand.oas'

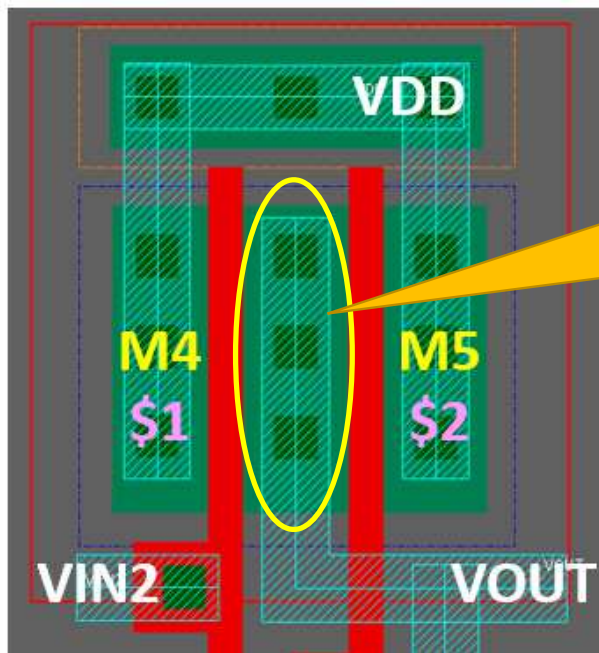
Top cell name = 'nand'

SPIICE deck file = 'nand-choice01.cir'



24. Summary and Further Questions

- ◆ In the case of the Inv and Inv2 LVS, all four reference netlists matched as expected with $S \leftrightarrow D$ swapping.
- ◆ In the case of the 2-input NAND, why does only PMOS M5 behave differently regarding the $S \leftrightarrow D$ swapping?



This region appears to be identified as

- the Drain of M4 (\$1)

as well as

- the Source of M5 (\$2)

24. Summary and Further Questions

◆ Once a certain combination is matched *by chance* (algorithm/input dependent), are no further possibilities (even if any) checked?



Matthias

February 13

@WENSHIH: source and drain are interchangeable in the standard MOS device. So that is not the problem here. KLayout will basically assign S and D randomly and try both ways during compare (and also during device combination).



Matthias

February 17

@dick_freebird About the S/D symmetry: the MOS3/MOS4 extractors are by design symmetric. As S/D are represented by the same layer, they cannot differentiate. So if the schematic is correct, there is no switch by which I can tell the extractors (hence the extracted netlist) to use a specific source/drain orientation. So no configuration option.
But the solution is simply to use DMOS3/DMOS4 for asymmetric devices (I think that can be clearly differentiated by the device type). If you do so, there are two separate layers for S and D, and there is no ambiguity.

Matthias

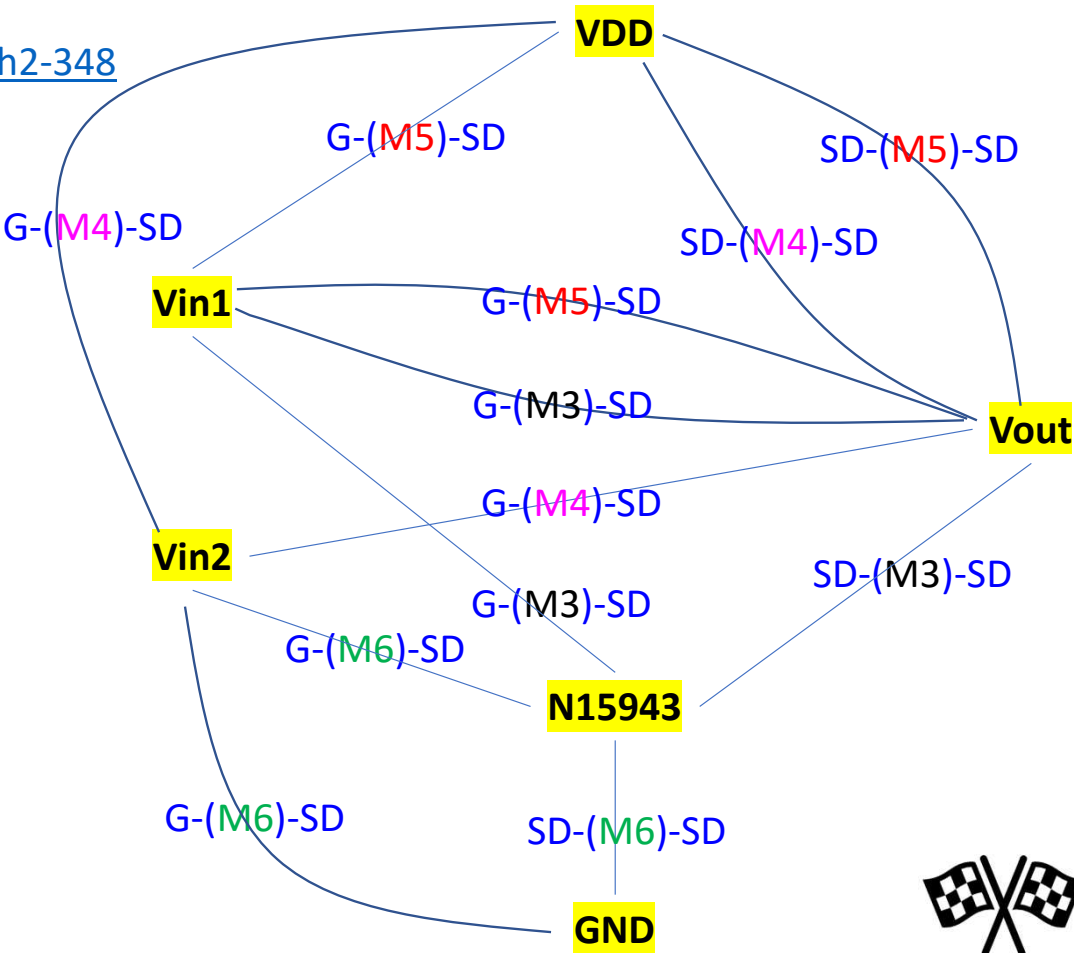
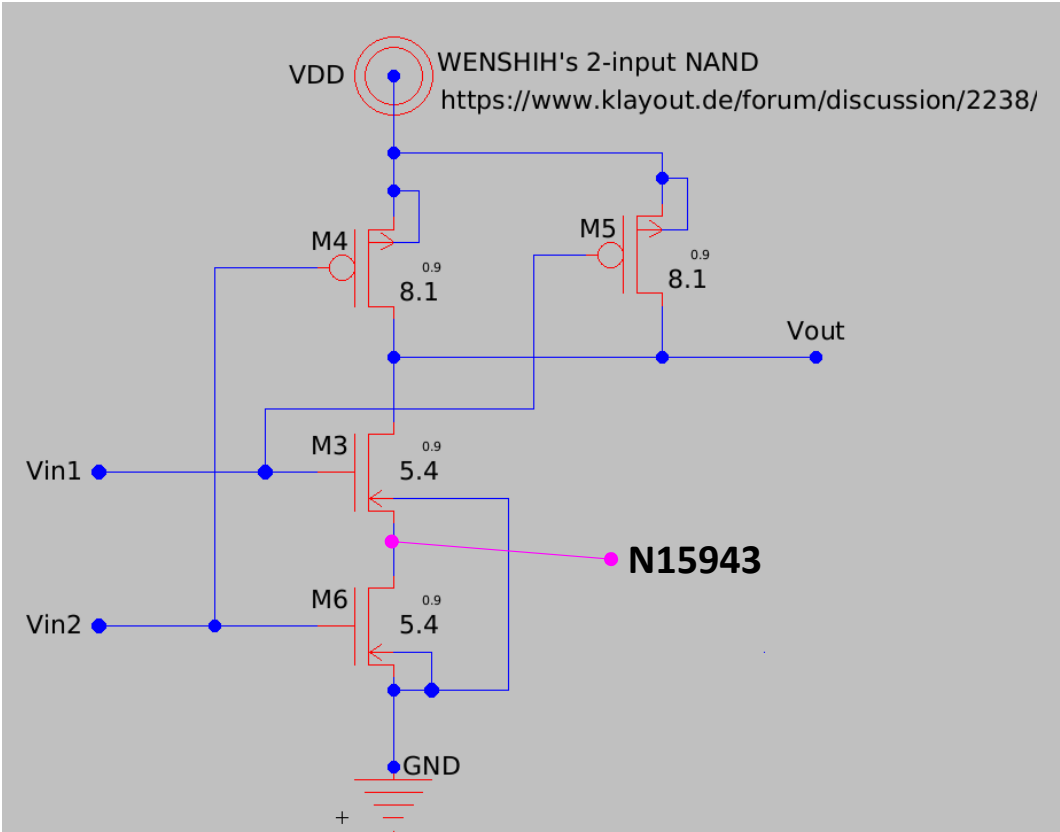
Already verified in “LVS-CMOS-Inverter-NAND-Con1.pptx”

Have I just confirmed this **specification** through this experiment?

24. Summary and Further Questions

◆ I have drawn the net neighborhood graph for the 2-input NAND for my study.

Ref. https://www.klayout.de/doc-qt5/manual/lvs_compare.html#h2-348



Local Parts Storeroom

