



LVS of CMOS Inverter and 2-input NAND

Aim:

To understand the basics of
KLayout's LVS

Disclaimer:

This document is for personal records only.
There is NO WARRANTY on technical
correctness.



By Kazzz-S (2023-02-21)

Part-I: Getting Started

Summary of My Confusion

1. Study Materials

[Main Index](#) » [KLayout User Manual](#) » Layout vs. Schematic (LVS)

Layout vs. Schematic (LVS)

LVS is a verification step which checks whether a layout matches the circuit from the schematic. The LVS feature is described in the following topic chapters:

- [Layout vs. Schematic \(LVS\) Overview](#)
- [LVS Introduction](#)
- [LVS Devices](#)
- [LVS Device Classes](#)
- [LVS Device Extractors](#)
- [LVS Input/Output](#)
- [LVS Connectivity](#)
- [LVS Compare](#)
- [LVS Netlist Tweaks](#)



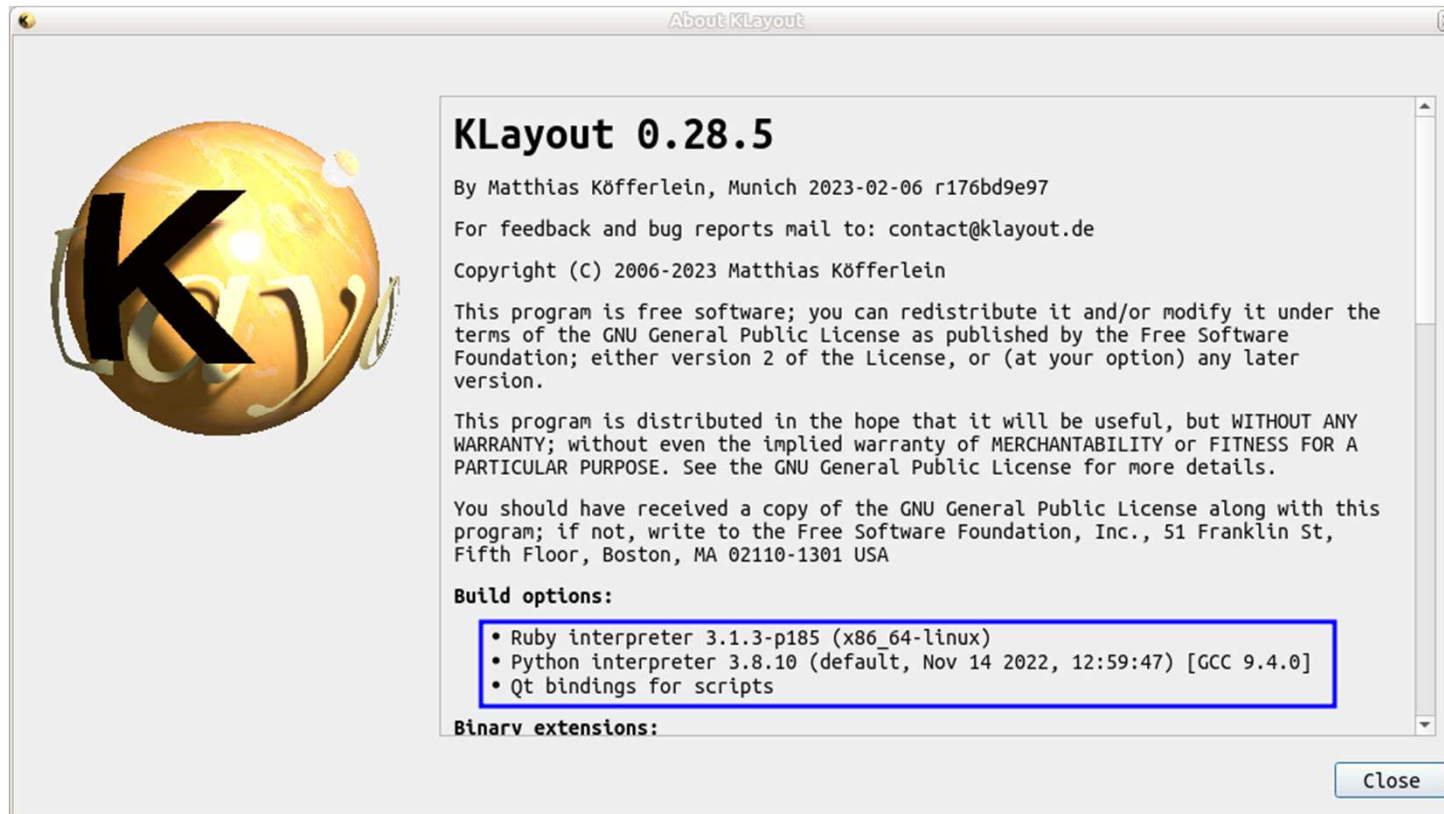
A reference for the functions and objects available for LVS scripts can be found here: [LVS Reference](#).

Forum

[1] <https://www.klayout.de/forum/discussion/2234/net-check-on-package-level>

[2] <https://www.klayout.de/forum/discussion/2238/how-to-extract-transistor-in-parallel-topology-in-lvs>

2. Study Environment and Legends in this Document



Legends:

(1) my understandings/guesses

<1> my questions

3. Incorrect SPICE Net

<1> The original [inv.cir](#) and [inv2.cir](#) seem incorrect; or simple typos? ▶

inv.cir	Original/Incorrect	invKazzzS.cir	Modified/Correct
<pre>1 2 * Simple CMOS inverer circuit 3 4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD 5 Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U 6 Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U 7 .ENDS 8</pre>		<pre>1 2 * Simple CMOS inverter circuit 3 4 * Original: \${klayout_root}/testdata/lvs/inv.cir 5 6 * Modified: invKazzzS.cir 7 * by: Kazzz-S 8 * date: 2023-02-07 9 * reasons: Terminals (drain and source) of the PMOS seem interchanged 10 11 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD 12 * Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U 13 Mp OUT IN VDD NWELL PMOS W=1.5U L=0.25U 14 Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U 15 .ENDS</pre>	
<pre>1 2 * Simple CMOS inverer circuit 3 4 .SUBCKT INVERTER WITH DIODES VSS IN OUT VDD 5 Mp VDD IN OUT VDD PMOS W=1.5U L=0.25U 6 Mn OUT IN VSS VSS NMOS W=0.9U L=0.25U 7 .ENDS 8</pre>		<pre>1 2 * Simple CMOS inverter circuit 3 4 * Original: \${klayout_root}/testdata/lvs/inv2.cir 5 6 * Modified: inv2KazzzS.cir 7 * by: Kazzz-S 8 * date: 2023-02-10 9 * reasons: Terminals (drain and source) of the PMOS seem interchanged 10 11 .SUBCKT INVERTER WITH DIODES VSS IN OUT VDD 12 * Mp VDD IN OUT VDD PMOS W=1.5U L=0.25U 13 Mp OUT IN VDD VDD PMOS W=1.5U L=0.25U 14 Mn OUT IN VSS VSS NMOS W=0.9U L=0.25U 15 .ENDS</pre>	

3. Incorrect SPICE Net

- (1) PMOS' swapped drain-source connections in the reference SPICE nets could be **intentional** to test the internal algorithm of LVS because in the Forum [2] ...



Matthias

6:53AM on 2023-02-13

@WENSHIH: source and drain are interchangeable in the standard MOS device. So that is not the problem here. KLayout will basically assign S and D randomly and try both ways during compare (and also during device combination).

"combine_devices" will not have an effect as there are no parallel devices as @dick_freebird pointed out.

Could you show us your schematic netlist? After all, this is a simple NAND, so that should actually be very simple.

Matthias

3. Incorrect SPICE Net

<2> Then, why do both extracted (resultant) nets coincide but are incorrect (drain and source interchanged)?

inv_extracted.cir

1 * Extracted by KLayout
2
3 * cell INVERTER
4 .SUBCKT INVERTER
5 * net 1 IN
6 * net 2 VSS
7 * net 3 VDD
8 * net 4 OUT
9 * net 5 NWELL
10 * net 6 SUBSTRATE
11 * device instance \$1 r0 *1 1.025,4.95 PMOS
12 M\$1 3 1 4 5 PMOS L=0.25U W=1.5U AS=0.675P AD=0.675P PS=3.9U PD=3.9U
13 * device instance \$2 r0 *1 1.025,0.65 NMOS
14 M\$2 2 1 4 6 NMOS L=0.25U W=0.9U AS=0.405P AD=0.405P PS=2.7U PD=2.7U
15 .ENDS INVERTER

inv_extracted_KazzzS.cir

1 * Extracted by KLayout with <invKazzzS.cir>
2
3 * cell INVERTER
4 .SUBCKT INVERTER
5 * net 1 IN
6 * net 2 VSS
7 * net 3 VDD
8 * net 4 OUT
9 * net 5 NWELL
10 * net 6 SUBSTRATE
11 * device instance \$1 r0 *1 1.025,4.95 PMOS
12 M\$1 3 1 4 5 PMOS L=0.25U W=1.5U AS=0.675P AD=0.675P PS=3.9U PD=3.9U
13 * device instance \$2 r0 *1 1.025,0.65 NMOS
14 M\$2 2 1 4 6 NMOS L=0.25U W=0.9U AS=0.405P AD=0.405P PS=2.7U PD=2.7U
15 .ENDS INVERTER

inv2_extracted.cir

1 * Extracted by KLayout
2
3 * cell INVERTER_WITH_DIODES
4 .SUBCKT INVERTER_WITH_DIODES
5 * net 1 IN
6 * net 2 VDD
7 * net 3 OUT
8 * net 4 VSS
9 * device instance \$1 r0 *1 1.025,4.95 PMOS
10 M\$1 2 1 3 2 PMOS L=0.25U W=1.5U AS=0.675P AD=0.675P PS=3.9U PD=3.9U
11 * device instance \$2 r0 *1 1.025,0.65 NMOS
12 M\$2 4 1 3 4 NMOS L=0.25U W=0.9U AS=0.405P AD=0.405P PS=2.7U PD=2.7U
13 .ENDS INVERTER_WITH_DIODES

inv2_extracted_KazzzS.cir

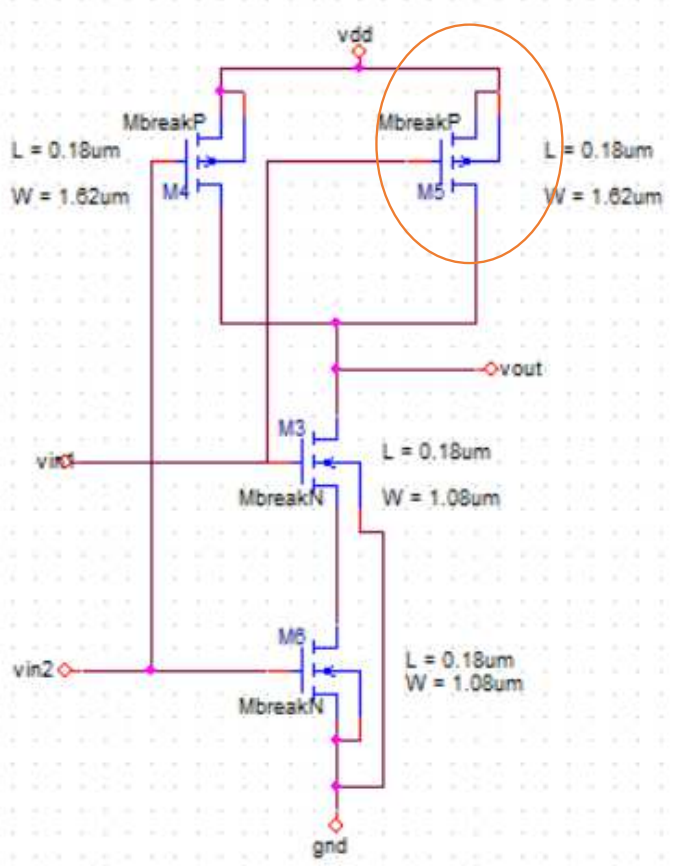
1 * Extracted by KLayout with <inv2KazzzS.cir>
2
3 * cell INVERTER_WITH_DIODES
4 .SUBCKT INVERTER_WITH_DIODES
5 * net 1 IN
6 * net 2 VDD
7 * net 3 OUT
8 * net 4 VSS
9 * device instance \$1 r0 *1 1.025,4.95 PMOS
10 M\$1 2 1 3 2 PMOS L=0.25U W=1.5U AS=0.675P AD=0.675P PS=3.9U PD=3.9U
11 * device instance \$2 r0 *1 1.025,0.65 NMOS
12 M\$2 4 1 3 4 NMOS L=0.25U W=0.9U AS=0.405P AD=0.405P PS=2.7U PD=2.7U
13 .ENDS INVERTER_WITH_DIODES

4. Another Sample of Incorrect SPICE Net

Incorrect. Exported by the schematic capture tool?
Or manually edited for testing? See slide #9 - #11.

WENSHIH
February 13 edited 12:14AM on 2023-02-14

Here is my schematic and schematic netlist.



```
.SUBCKT nand VDD GND VIN1 VIN2 VOUT
M_M6 GND VIN2 N15943 GND MbreakN L=0.18um W=1.08um
M_M3 N15943 VIN1 VOUT GND MbreakN L=0.18um W=1.08um
M_M5 VDD VIN1 VOUT VDD MbreakP L=0.18um W=1.62um
M_M4 VDD VIN2 VOUT VDD MbreakP L=0.18um W=1.62um
.ENDS
```

missing! not required?

Does it mean the LVS of layout would identify the mos that S and D are opposite in pair?
Like below. M5 is from the schematic netlist \$2 is from the layout netlist.

correct

- MBRE/M5
 - S VDD (4)
 - D VOUT (3)
 - G VIN1 (2)
 - B VDD (4)

correct

- Mbreak\$2
 - S vout (4)
 - D vdd (5)
 - G vin1 (3)
 - B vdd (5)

incorrect

Could you please explain more about fully parallel?
Thanks!
WENSHIH



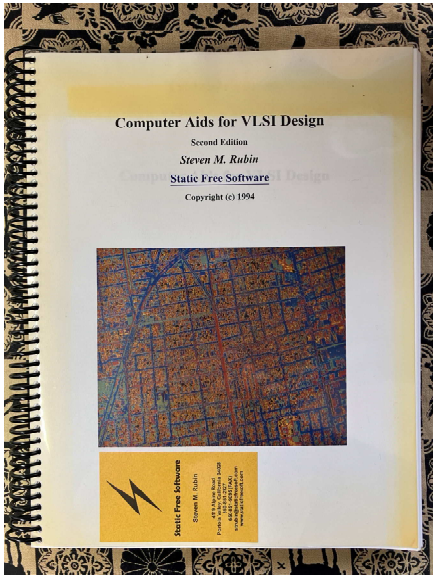
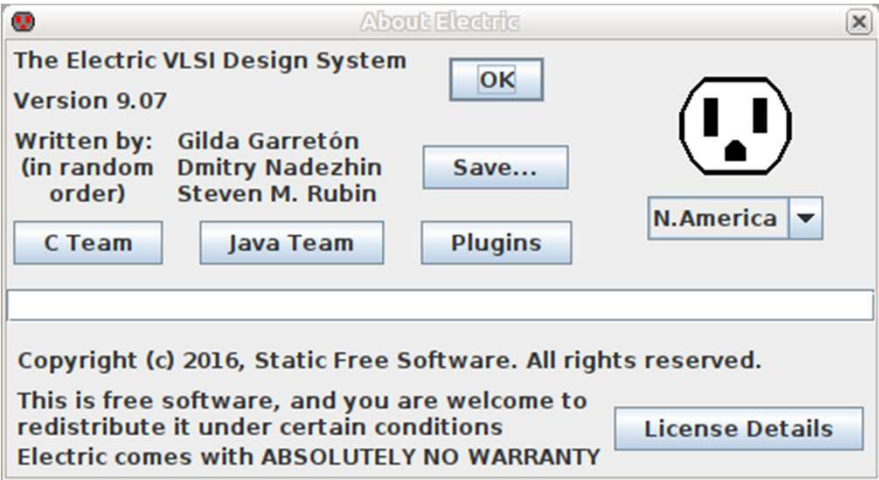
4. Another Sample of Incorrect SPICE Net

- Correct (expected) SPICE net to be extracted

```
.SUBCKT nand VDD GND VIN1 VIN2 VOUT
M_M6 N15943 VIN2 GND GND MbreakN L=0.18um W=1.08um
M_M3 VOUT VIN1 N15943 GND MbreakN L=0.18um W=1.08um
M_M5 VOUT VIN1 VDD VDD MbreakP L=0.18um W=1.62um
M_M4 VOUT VIN2 VDD VDD MbreakP L=0.18um W=1.62um
.ENDS
```

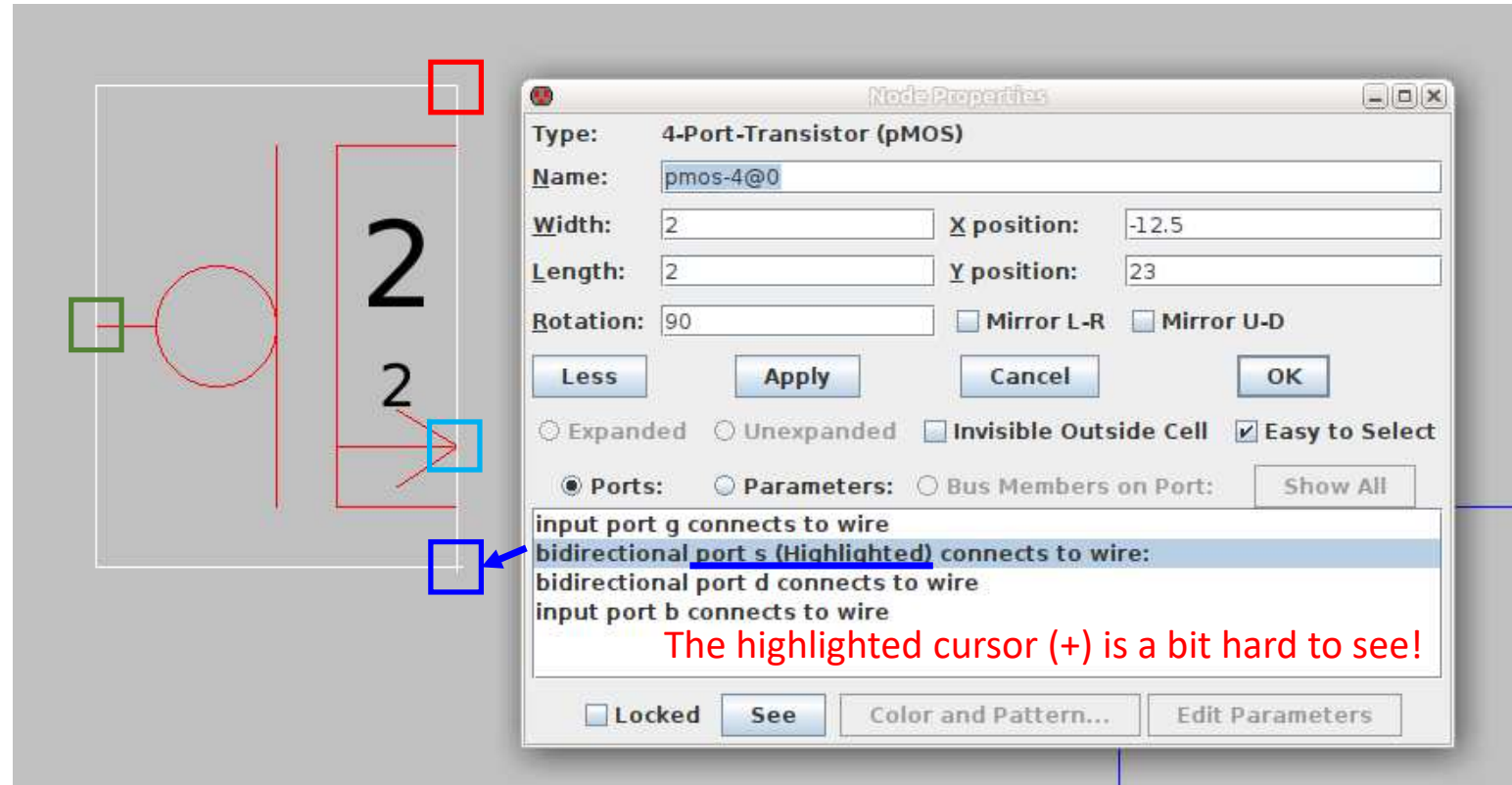
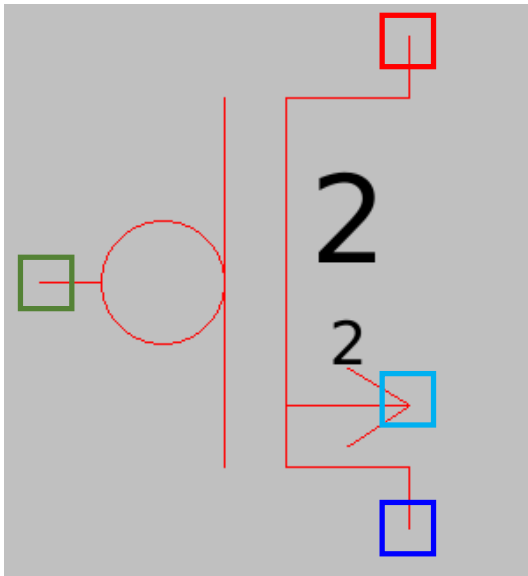
Extracting a correct SPICE deck is a duty of a schematic editor, not of KLayout!

- Let's try the **Electric** CAD (developed by the legendary Steven M. Rubin) after many many many years!

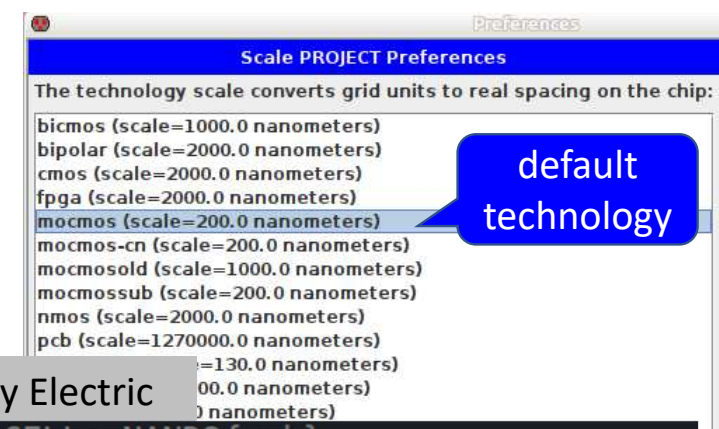
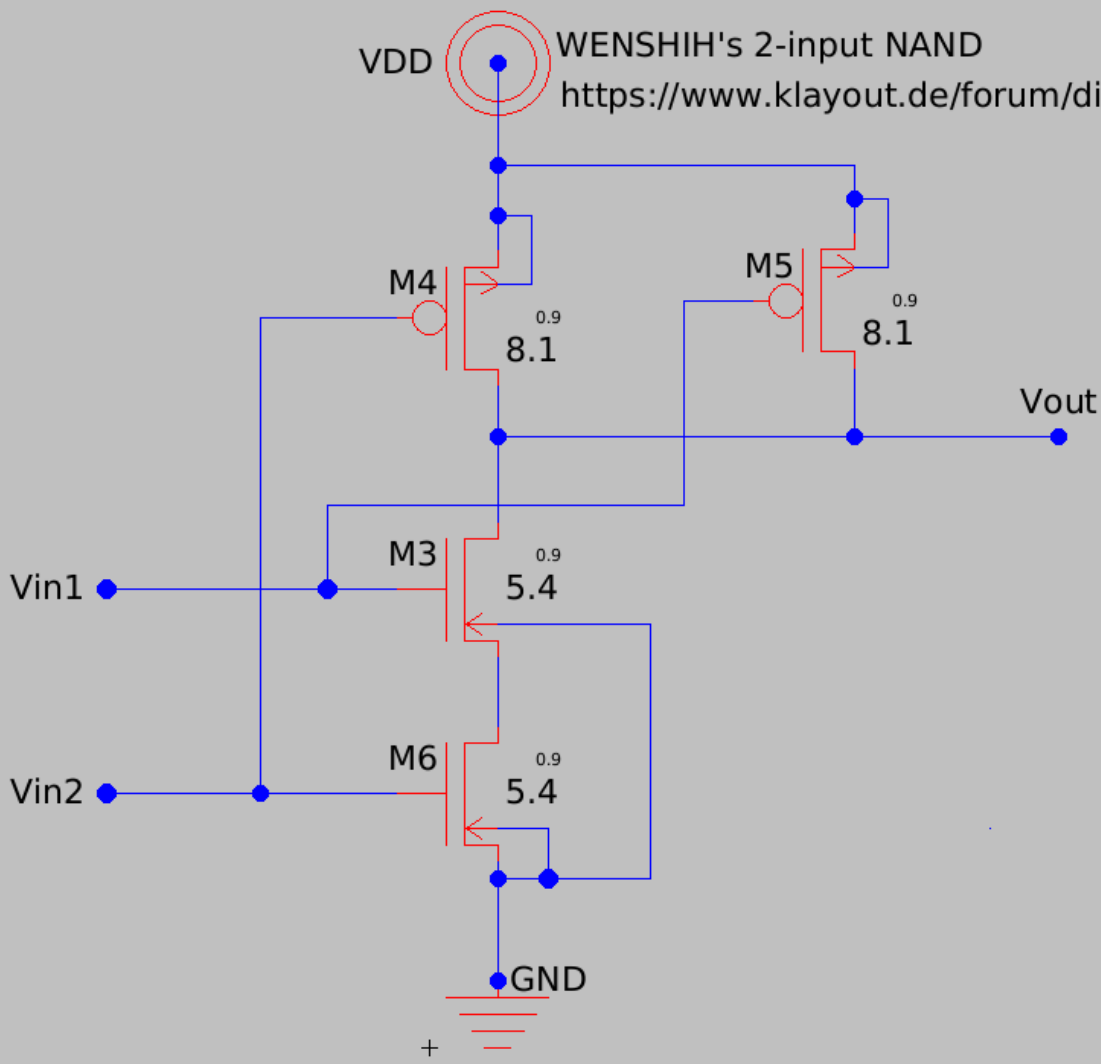


4. Another Sample of Incorrect SPICE Net

- Schematic symbol of a PMOS and its four terminals (ports) in *Electric*
- The **source** is closer to the **bulk**; the symbol is asymmetric to avoid misconnection.



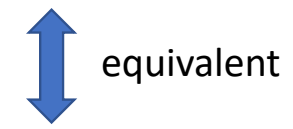
4. Another Sample of Incorrect SPICE Net



SPICE net exported by Electric

```
21 *** TOP LEVEL CELL: NAND2{sch}
22 MM6 net@94 Vin2 GND GND N L=0.18U W=1.08U
23 MM3 Vout Vin1 net@94 GND N L=0.18U W=1.08U
24 MM5 Vout Vin1 VDD VDD P L=0.18U W=1.62U
25 MM4 Vout Vin2 VDD VDD P L=0.18U W=1.62U
26 .END
27
28
```

The row order has been changed.



Correct (expected) SPICE net

```
.SUBCKT nand VDD GND VIN1 VIN2 VOUT
M_M6 N15943 VIN2 GND GND MbreakN L=0.18um W=1.08um
M_M3 VOUT VIN1 N15943 GND MbreakN L=0.18um W=1.08um
M_M5 VOUT VIN1 VDD VDD MbreakP L=0.18um W=1.62um
M_M4 VOUT VIN2 VDD VDD MbreakP L=0.18um W=1.62um
.ENDS
```

5. Incorrect Device Terminal Connections

<3> The device connections are more confusing because...

inv.lvsubd

with original incorrect reference net

invKazzzS.lvsubd

with modified correct reference net

180 net(5 name(SUBSTRATE))
181 net(6 name(VDD))
182
183 # Outgoing pins and their connections to nets
184 pin(1 name(VSS))
185 pin(2 name(IN))
186 pin(3 name(OUT))
187 pin(4 name(NWELL))
188 pin(5 name(SUBSTRATE))
189 pin(6 name(VDD))
190
191 # Devices and their connections
192 device(1 PMOS
193 name(P)
194 param(L 0.25)
195 param(W 1.5)
196 param(AS 0)
197 param(AD 0)
198 param(PS 0)
199 param(PD 0)
200 terminal(S 6)
201 terminal(G 2)
202 terminal(D 3)
203 terminal(B 4)
204)
205 device(2 NMOS
206 name(N)
207 param(L 0.25)
208 param(W 0.9)
209 param(AS 0)
210 param(AD 0)
211 param(PS 0)
212 param(PD 0)
213 terminal(S 3)
214 terminal(G 2)
215 terminal(D 1)
216 terminal(B 5)
217)

correct

incorrect

180 net(5 name(SUBSTRATE))
181 net(6 name(VDD))
182
183 # Outgoing pins and their connections to nets
184 pin(1 name(VSS))
185 pin(2 name(IN))
186 pin(3 name(OUT))
187 pin(4 name(NWELL))
188 pin(5 name(SUBSTRATE))
189 pin(6 name(VDD))
190
191 # Devices and their connections
192 device(1 PMOS
193 name(P)
194 param(L 0.25)
195 param(W 1.5)
196 param(AS 0)
197 param(AD 0)
198 param(PS 0)
199 param(PD 0)
200 terminal(S 3)
201 terminal(G 2)
202 terminal(D 6)
203 terminal(B 4)
204)
205 device(2 NMOS
206 name(N)
207 param(L 0.25)
208 param(W 0.9)
209 param(AS 0)
210 param(AD 0)
211 param(PS 0)
212 param(PD 0)
213 terminal(S 3)
214 terminal(G 2)
215 terminal(D 1)
216 terminal(B 5)
217)

incorrect

incorrect

to be cont.

KLayout Forum No. 2238 (as Study002: LVS of CMOS Inverter and 2-input NAND)

12

5. Incorrect Device Terminal Connections

cont.

inv2.lvstdbwith original incorrect reference net

```
189 .net(1 name(VSS))
190 .net(2 name(IN))
191 .net(3 name(OUT))
192 .net(4 name(VDD))
193
194 # Outgoing pins and their connections to nets
195 .pin(1 name(VSS))
196 .pin(2 name(IN))
197 .pin(3 name(OUT))
198 .pin(4 name(VDD))
199
200 # Devices and their connections
201 .device(1 PMOS
202 .name(P)
203 .param(L 0.25)
204 .param(W 1.5)
205 .param(AS 0)
206 .param(AD 0)
207 .param(PS 0)
208 .param(PD 0)
209 .terminal(S 4)
210 .terminal(G 2)
211 .terminal(D 3)
212 .terminal(B 4)
213 )
214 .device(2 NMOS
215 .name(N)
216 .param(L 0.25)
217 .param(W 0.9)
218 .param(AS 0)
219 .param(AD 0)
220 .param(PS 0)
221 .param(PD 0)
222 .terminal(S 3)
223 .terminal(G 2)
224 .terminal(D 1)
225 .terminal(B 1)
226 )
227
228 )
```

correct

incorrect

inv2KazzzS.lvstdbwith modified correct reference net

```
189 .net(1 name(VSS))
190 .net(2 name(IN))
191 .net(3 name(OUT))
192 .net(4 name(VDD))
193
194 # Outgoing pins and their connections to nets
195 .pin(1 name(VSS))
196 .pin(2 name(IN))
197 .pin(3 name(OUT))
198 .pin(4 name(VDD))
199
200 # Devices and their connections
201 .device(1 PMOS
202 .name(P)
203 .param(L 0.25)
204 .param(W 1.5)
205 .param(AS 0)
206 .param(AD 0)
207 .param(PS 0)
208 .param(PD 0)
209 .terminal(S 3)
210 .terminal(G 2)
211 .terminal(D 4)
212 .terminal(B 4)
213 )
214 .device(2 NMOS
215 .name(N)
216 .param(L 0.25)
217 .param(W 0.9)
218 .param(AS 0)
219 .param(AD 0)
220 .param(PS 0)
221 .param(PD 0)
222 .terminal(S 3)
223 .terminal(G 2)
224 .terminal(D 1)
225 .terminal(B 1)
226 )
227
228 )
```

incorrect

incorrect

6. Correct Cross-References

<4> The cross-references are much more confusing because all seem **correct eventually** but are inconsistent with the other (intermediate) results. Where are my misunderstandings?

Netlist Schematic Cross Reference Log

Circuits

INVERTER

Objects

INVERTER

Layout

INVERTER

Reference

INVERTER

with original incorrect reference net

correct

\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]

VSS (1) VSS (2)

OUT (2) OUT (3)

IN (2) IN (3)

SUBSTRATE (1) SUBSTRATE (2)

\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]

VDD (1) VDD (2)

OUT (2) OUT (3)

IN (2) IN (3)

NWELL (1) NWELL (2)

Netlist Schematic Cross Reference Log

Circuits

INVERTER

Objects

INVERTER

Layout

INVERTER

Reference

INVERTER

with modified correct reference net

correct

\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]

VSS (1) VSS (2)

OUT (2) OUT (3)

IN (2) IN (3)

SUBSTRATE (1) SUBSTRATE (2)

\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]

VDD (1) VDD (2)

OUT (2) OUT (3)

IN (2) IN (3)

NWELL (1) NWELL (2)

to be cont.

6. Correct Cross-References

Netlist Schematic Cross Reference Log

Circuits

INVERTER_WITH_DIODES

cont.

Objects

INVERTER_WITH_D

Layout

Reference

INVERTER_WITH_DIODES

with original incorrect reference net

correct

\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]

VSS (2) VSS (3)

OUT (2) OUT (3)

IN (2) IN (3)

VSS (2) VSS (3)

\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]

VDD (2) VDD (3)

OUT (2) OUT (3)

IN (2) IN (3)

VDD (2) VDD (3)

Log

Circuits

INVERTER_WITH_DIODES

Layout

Reference

INVERTER_WITH_DIO

with modified correct reference net

correct

\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]

VSS (2) VSS (3)

OUT (2) OUT (3)

IN (2) IN (3)

VSS (2) VSS (3)

\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]

VDD (2) VDD (3)

OUT (2) OUT (3)

IN (2) IN (3)

VDD (2) VDD (3)

7. Netlist Database Browser

<5> Is there any detailed document interpreting each item that could appear in the netlist database browser? I've tried to find it but couldn't so far. Some items are very intuitive. However, others are not.

<5b> Does **Schematic** mean the netlist extracted from the reference SPICE deck and correspond to **Reference**?

(2) Extracted from the layout [inv.oas](#)

(3) Extracted from the reference net [inv.cir](#)

<5a> Does **Netlist** mean the netlist extracted from the layout and correspond to **Layout**?

<5c> What does \Leftrightarrow symbol mean?

Log is empty in this case. However, there would be something to point out such as the incorrect reference SPICE net.

<5d> What does a number in () mean?

Part-II: Digesting the Discussions

8. Interchangeability of Source and Drain in the Standard MOS Device

- I believe part of my confusion stems from my understanding of **source and drain interchangeability**.



Matthias

6:53AM on 2023-02-13

To me, this is not always correct.

@WENSHIH: source and drain are interchangeable in the standard MOS device. So that is not the problem here. KLayout will basically assign S and D randomly and try both ways during compare (and also during device combination).

"combine_devices" will not have an effect as there are no parallel devices as @dick_freebird pointed out.

Could you show us your schematic netlist? After all, this is a simple NAND, so that should actually be very simple.

Matthias

8. Interchangeability of Source and Drain in the Standard MOS Device



Matthias

2:17AM on 2023-02-20

@sekigawa Thanks for these elaborate slides!

I should comment about the "correctness" here: my viewpoint is that "S" and "D" for a symmetric device should both be read as "S or D" as there is no differentiation.

Sure the schematic is not correct if you tie D to vdd, but S and D are only logical concepts for symmetric devices. You could say that for a PMOS, D is the terminal with the lower and S is the terminal with the higher potential. For NMOS it is the other way round.

I guess that for simulation, the models do not necessarily reflect that symmetry, so for that practical reason it is probably better to assign D and S correctly in the schematic. At least if you want to use this netlist for simulation. For the topology however, the assignment is not binding for symmetric devices.

Lacking any differentiating marker, the layout extractor on the other hand will arbitrarily assign S and D for symmetric devices (like said, both terminals should be regarded "S or D"). It does not take any efforts correcting this "mistake". Instead, the netlist *compare* step regards "S" and "D" as interchangeable, hence the netlists match and all cases.

For DMOS3/4 class devices, the extractor can tell apart S and D and the netlist comparer will no longer regard S and D as interchangeable.

Matthias

This is a very important tool design concept, and I respect it. However, I could not read it from the inverter tutorials.

Moreover, influenced by my previous experiences, I have a different view (#20 - #24) on "S and D," which created a fundamental gap that caused my confusion.

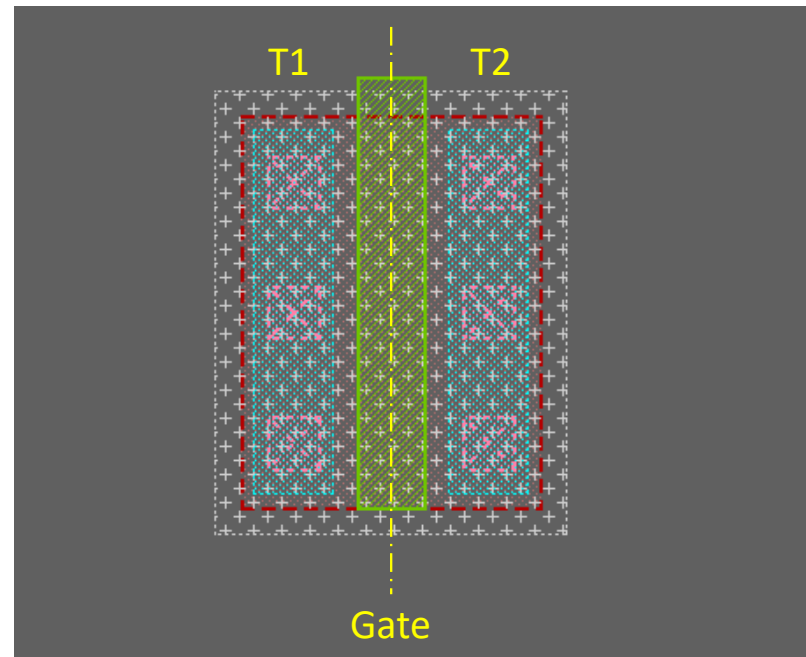
8. Interchangeability of Source and Drain in the Standard MOS Device

- Below is a layout of a floating PMOS that is geometrically symmetry with respect to the gate poly.
- The terminals T1 and T2 can become the source and drain, or the drain and source, respectively.
- Therefore, we say ***“the source and drain can be interchangeable.”***
 - No objection in this stage.
- In other words, however, we cannot identify which is the source and which is the drain.

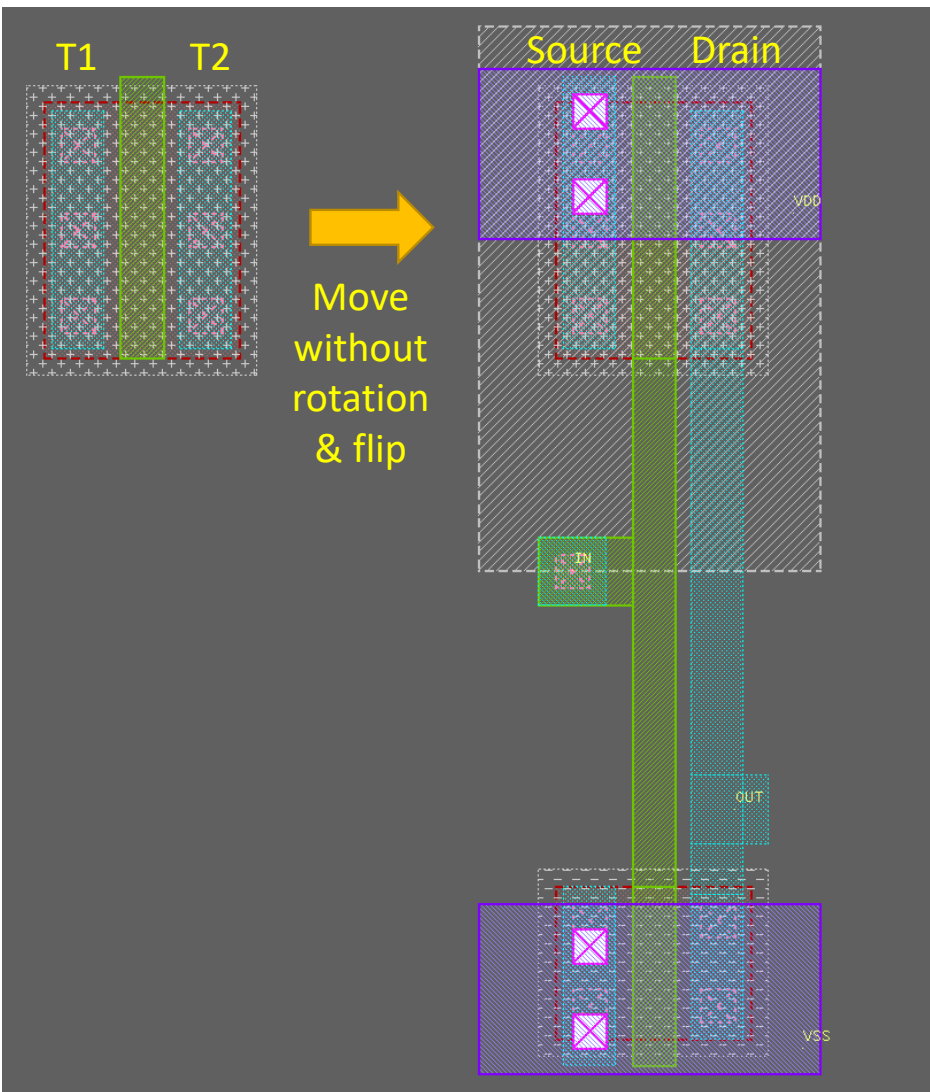
I should comment about the "correctness" here: my viewpoint is that "S" and "D" for a symmetric device should both be read as "S or D" as there is no differentiation.



We agree so far!



8. Interchangeability of Source and Drain in the Standard MOS Device



- Once the PMOS is used/connected in an Inverter, **ambiguity vanishes**.
- That is, **T1** is forcibly given the generic name of **Source**; **T2**, **Drain**
- Then, **Source** and **Drain** are no longer interchangeable in the Inverter.*
- And the SPICE net must be as follows; no other terminal connection can be possible as an Inverter.





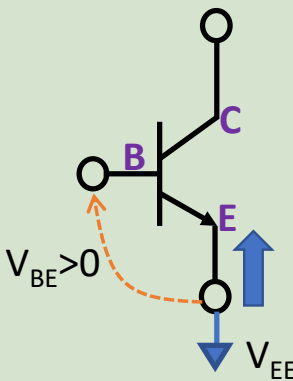
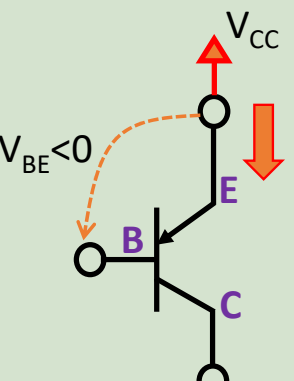
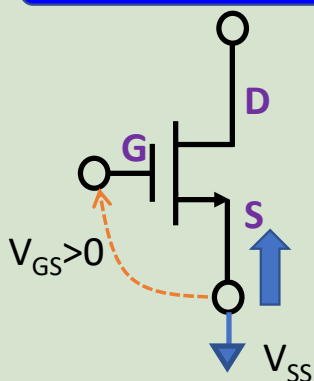
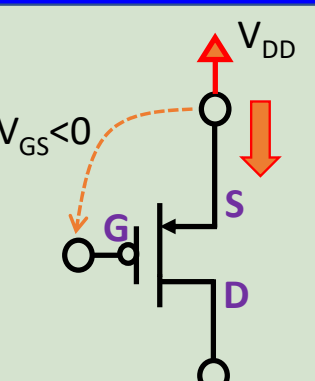
```
1
2  * Simple CMOS inverter circuit
3  *
4  * Original: ${klayout_root}/testdata/lvs/inv.cir
5  *
6  * Modified: invKazzzS.cir
7  *   by: Kazzz-S
8  *   date: 2023-02-07
9  *   reasons: Terminals (drain and source) of the PMOS seem interchanged
10
11  .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
12  * Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
13  Mp OUT IN VDD NWELL PMOS W=1.5U L=0.25U
14  Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U
15  .ENDS
```

Drain Source

SPICE is for simulating the behavior of circuitry.

(*) **Source** and **Drain** are the names of geometrical regions in the mask layout, of course. At the same time, more importantly, they imply the physical roles or behaviors in circuitry. Refer to the next slide.

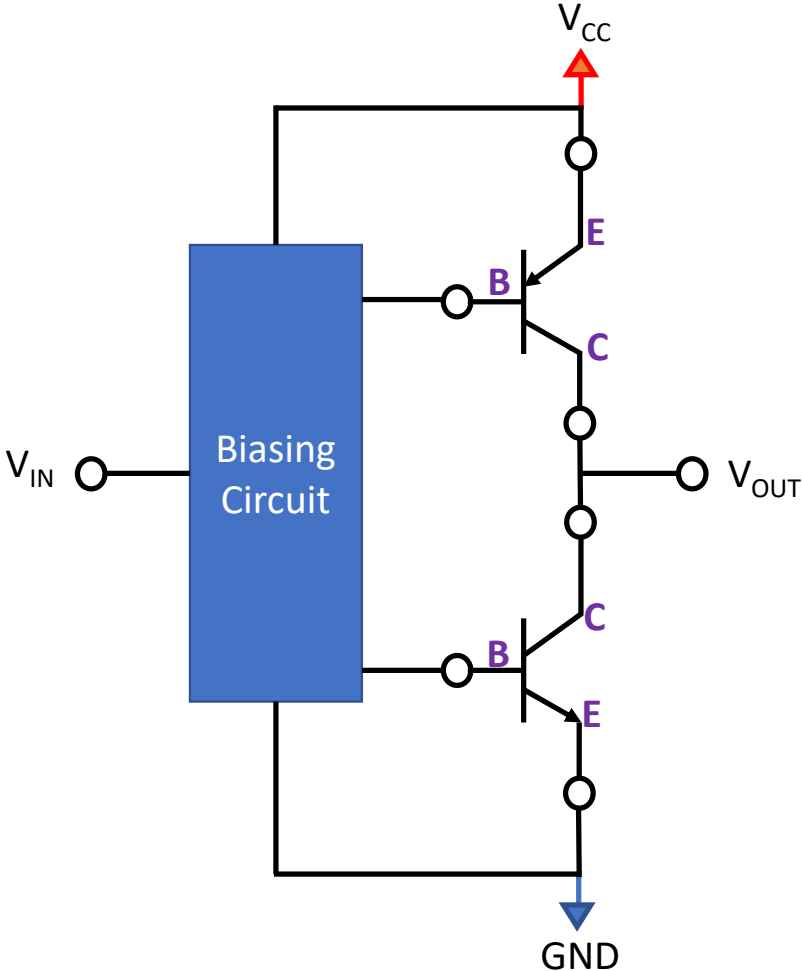
9. My Understandings on Semiconductor Devices

Device	NPN BJT	PNP BJT	N-ch MOS Tr	P-ch MOS Tr
Physics				
Majority Carrier	Electron 	Hole 	Electron 	Hole 
* Majority Carrier Injector (Pitcher)	Emitter	Emitter	Source	Source
* Majority Carrier Controller	Base-Emitter Voltage ($V_{BE}>0$)	Base-Emitter Voltage ($V_{BE}<0$)	Gate-Source Voltage ($V_{GS}>0$)	Gate-Source Voltage ($V_{GS}<0$)
* Majority Carrier Receiver (Catcher)	Collector	Collector	Drain	Drain
Circuitry				

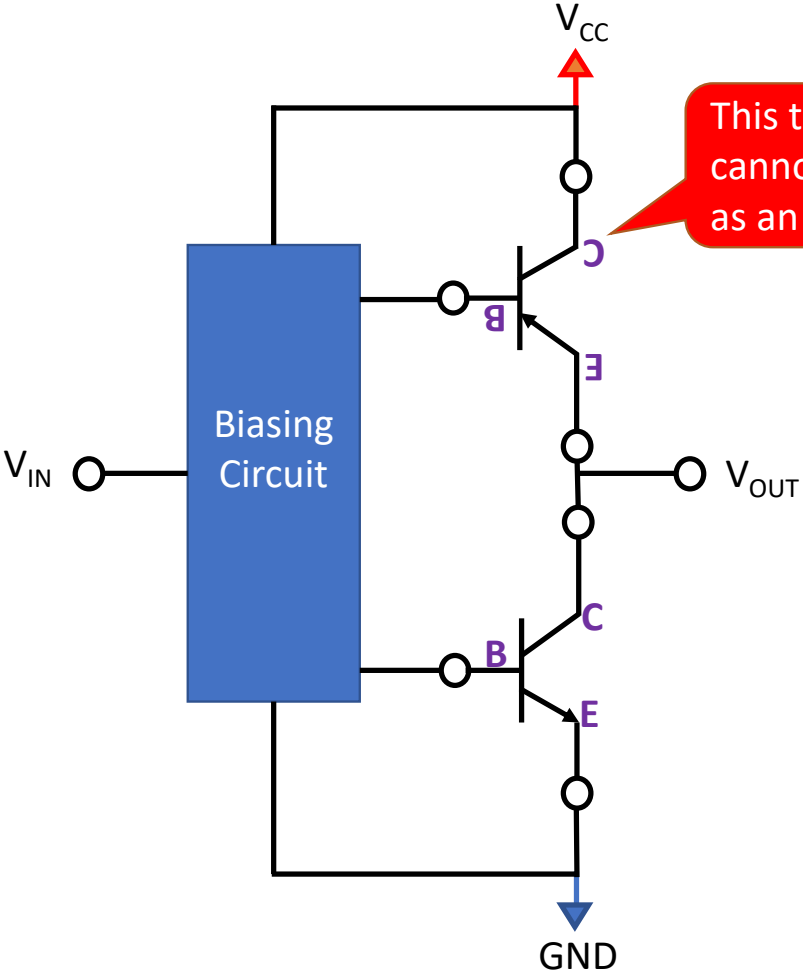
S and D are not logical but physical concepts

* My terminology **Old aphorism among BJT chip designers: *Emitter current decides everything.***

10. Interchangeability of Emitter and Collector in the BJT Device? No Way!



Will work with an appropriate biasing circuit



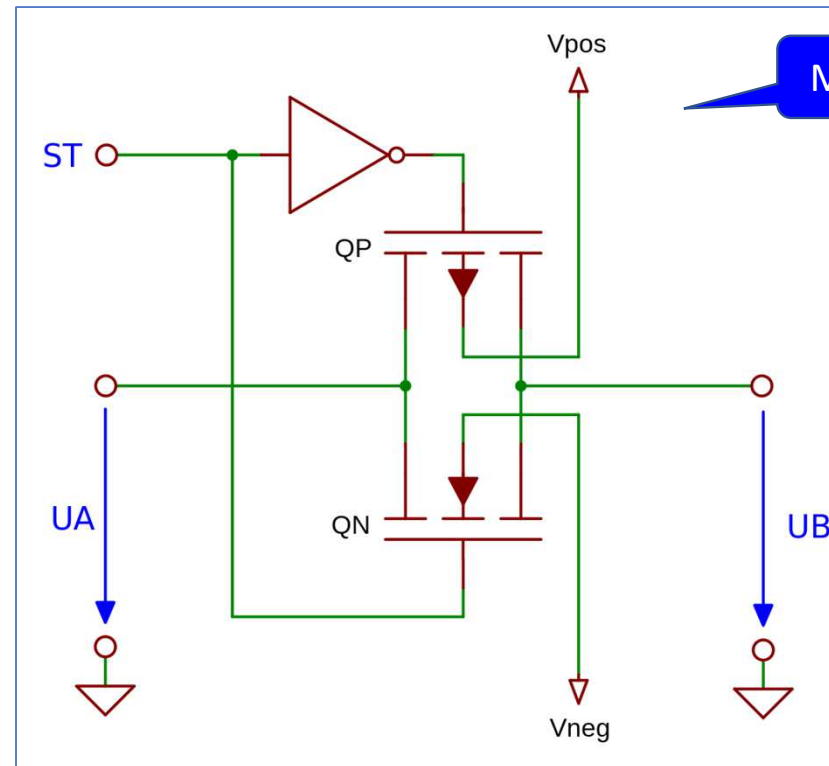
This terminal cannot work as an emitter



Won't work at all
Schematic itself is incorrect

11. Interchangeability of Source and Drain in the Standard MOS Device (again)

<6> In the Transmission Gate (analog switch) configuration, the Source and Drain names (and functions) are swappable. Is present KLayout's LVS designed to support this case?



Part-III: Experiments

- ◆ The original tutorials using [inv.cir](#) and [inv2.cir](#) seem not suitable as a “Hello, World!” program for LVS.
- ◆ They look simple at first glance but need a deep understanding of the LVS tool design concept.
- ◆ That is the pitfall I felt in.
- ◆ I prefer to pay an extra price for the overall simplicity and clarity of start something new.



12. Using DMOS4



Matthias

6:30AM on 2023-02-16

@dick_freebird I'm aware of this 😊

There is another model, called "DMOS3" (no bulk pin) and "DMOS4" (bulk pin) which treats source and drain separately (see https://www.klayout.de/doc-qt5/manual/lvs_device_extractors.html#h2-192). The price to pay is that you need separate recognition layers for source and drain.

The way I implement swapping is that for "MOS3" and "MOS4" I treat the schematic netlist as given (even if drain is on VDD or GND) and try both ways of the extracted device until a match is found. For "DMOS3" and "DMOS4" the latter step is skipped.

@WENSHIH Just sharing screenshots does not make sense. This is a simple case and no device combination is needed - that only applies to fingered devices which are in parallel (B, S, G and D share the same net). I don't see how the mismatch happens (LVS report), but I also don't see the script, I can't check the layers and derivations and I cannot measure the device dimensions as I do not have the layouts. I can't really help in that case.

Matthias



answer to

<1>

<6>

12. Using DMOS4



dick_freebird on 2023-02-20

5:15AM

Yes, they should be but evidently are not, and I am wanting to get to the bottom of "why?".

I figure maybe removing known "not-right" from input netlists might help expose the unknown.

Which thus far, remains unknown.

Let me ask another question which I have not seen specifically asked: "Which of the MOS extractors are in fact being used?".

It appears to me that this layout is done on a "found PDK" and perhaps somebody set it up with non-swapping extractors by default? If you poke into the devices do you find evidence that D, S are being force-assigned (the recognition layers mentioned)?

Corrolary activity: If MOS3 / MOS4 -are- being used, how about switching to DMOS3/4 and making the S/D symbol connections "correct"? Does that fix anything? Then if so, why?

I think that showing the extract deck and the layer objects of the NMOS and PMOS elements might offer clues. If there is any sort of report file generated during layout extraction, maybe that too?



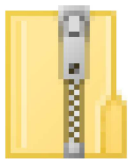
I agree with you!



I have already attempted this activity. Please go through the succeeding slides.

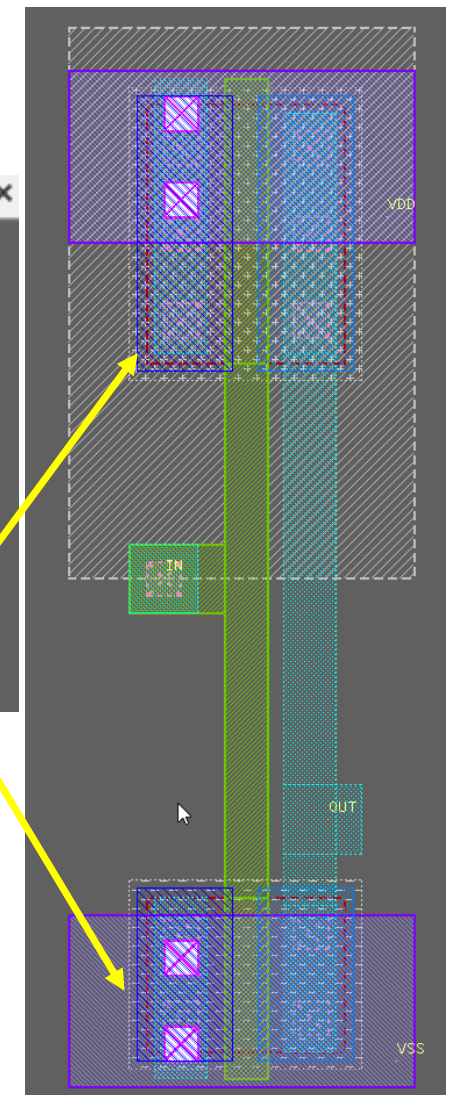
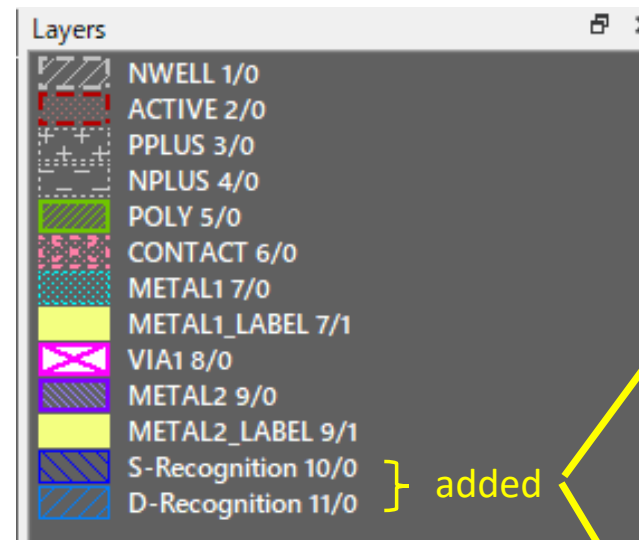
13. Using DMOS4 for the [inv.cir](#) Tutorial

1. Add two dummy layers to recognize S and D easily. They are logical instances.



All Files

Inv-DMOS4.zip



13. Using DMOS4 for the **inv.cir** Tutorial

2. Prepare four SPICE deck files to test all S and D combinations.

inv.cir x invX1.cir x invX2.cir x inv-DMOS4.cir x

```
1 |
2 | * Simple CMOS inverter circuit : original: (PMOS, NMOS)=(incorrect, correct)
3 |
4 | .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 | Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
6 | Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U
7 | .ENDS
8 |
```

\$choice=1

inv.cir x invX1.cir x invX2.cir x inv-DMOS4.cir x

```
1 |
2 | * Simple CMOS inverter circuit
3 | *
4 | * Original: ${klayout_root}/testdata/lvs/inv.cir
5 | *
6 | * Modified: inv-DMOS4.cir (PMOS, NMOS)=( correct, correct)
7 | * by: Kazzz-S
8 | * date: 2023-02-16
9 | * aims: 1) correct D-S connections of the PMOS (flipped in the original)
10 |
11 | .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
12 | * Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
13 | Mp OUT IN VDD NWELL PMOS W=1.5U L=0.25U
14 | Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U
15 | .ENDS
16 |
```

\$choice=4

I expect this should match!

inv.cir x invX1.cir x invX2.cir x inv-DMOS4.cir x

```
1 |
2 | * Simple CMOS inverter circuit: Variant X1: (PMOS, NMOS)=(incorrect, incorrect)
3 |
4 | .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 | Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
6 | Mn VSS IN OUT SUBSTRATE NMOS W=0.9U L=0.25U
7 | .ENDS
8 |
9 |
```

\$choice=2

inv.cir x invX1.cir x invX2.cir x inv-DMOS4.cir x

```
1 |
2 | * Simple CMOS inverter circuit: Variant X2: (PMOS, NMOS)=( correct, incorrect)
3 |
4 | .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 | Mp OUT IN VSS NWELL PMOS W=1.5U L=0.25U
6 | Mn VSS IN OUT SUBSTRATE NMOS W=0.9U L=0.25U
7 | .ENDS
8 |
9 |
```

\$choice=3

D and S are swapped

13. Using DMOS4 for the **inv.cir** Tutorial

3. Modify the sample LVS script for testing and debugging.

inv-DMOS4A.lvs

```
136 #-----
137 # [5] Device extraction
138 #-----
139 # PMOS transistor device extraction
140 extract_devices(dmos4("PMOS"), { "S"
141                                     "ts"
142                                     }
143 # NMOS transistor device extraction
144 extract_devices(dmos4("NMOS"), { "S"
145                                     "ts"
146                                     }
147 #-----
148 # [6] Define connectivity for netlist
149 #-----
150 # Inter-layer
151 connect(pss,      contact)
152 connect(pdd,      contact)
153 connect(nss,      contact)
154 connect(ndd,      contact)
155 connect(poly,     contact)
156 connect(contact,  metall)
157 connect(metall,   metall_lbl) # a
158 connect(metall,   vial)
159 connect(metall,   metal2)
160 connect(vial,     metal2)
161 connect(metal2,   metal2_lbl) # a
162 # Global
163 connect_global(bulk, "SUBSTRATE")
164 connect_global(nwell, "NWEELL")
165 #-----
166 # [7] Compare section
167 #-----
168 schematic(spicedeck)
169 compare
170 # EOF
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```

13. Using DMOS4 for the [inv.cir](#) Tutorial

4. Run the modified LVS script four times: #1/4

```
1 |
2 * Simple CMOS inverter circuit : original: (PMOS, NMOS)=(incorrect, correct)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
6 Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
```

\$choice=1

Netlist Schematic Cross Reference Log

Circuits

INVERTER

Objects

INVERTER

Pins

Nets

Devices

NMOS

S ↔ D

D ↔ S

G

B

PMOS

S

D

G

B

INVERTER

\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]

VSS (1)

OUT (2)

IN (2)

SUBSTRATE (1)

\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]

VDD (1)

OUT (2)

IN (2)

NWELL (1)

INVERTER

VSS (2)

OUT (3)

IN (3)

SUBSTRATE (2)

VDD (2)

OUT (3)

IN (3)

NWELL (2)

Configure Probe Net Lock

> \$choice=1

1

>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002/Inv-DMOS4/inv-DMOS4.oas'

Top cell name = 'INVERTER'

SPICE deck file = 'inv.cir'

13. Using DMOS4 for the **inv.cir** Tutorial

4. Run the modified LVS script four times: #2/4

```
1 |
2 * Simple CMOS inverter circuit: Variant X1: (PMOS, NMOS)=(incorrect, incorrect)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
6 Mn VSS IN OUT SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
9
```

\$choice=2

Only this matched!

Netlist Schematic Cross Reference Log

Circuits

INVERTER

Objects

INVERTER

Pins

Nets

Devices

NMOS

S

D

G

B

PMOS

S

D

G

B

Layout

INVERTER

Reference

INVERTER

Configure

Probe Net

Lock

> \$choice=2

2

>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002/Inv-DMOS4/inv-DMOS4.oas'

Top cell name = 'INVERTER'

SPICE deck file = 'invX1.cir'

13. Using DMOS4 for the [inv.cir](#) Tutorial

4. Run the modified LVS script four times: #3/4

```
1 |
2 * Simple CMOS inverter circuit: Variant X2: (PMOS, NMOS)=( correct, incorrect)
3
4 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
5 Mp OUT IN VSS NWELL PMOS W=1.5U L=0.25U
6 Mn VSS IN OUT SUBSTRATE NMOS W=0.9U L=0.25U
7 .ENDS
8
9
```

\$choice=3

Netlist Schematic Cross Reference Log

Circuits

Objects

Layout

Reference

INVERTER

INVERTER

INVERTER

INVERTER

Pins

Nets

Devices

NMOS

PMOS

\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]

OUT (2)

VSS (1)

IN (2)

SUBSTRATE (1)

\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]

VDD (1)

OUT (2)

IN (2)

NWELL (1)

VSS (3)

OUT (3)

IN (3)

SUBSTRATE (2)

OUT (3)

VSS (3)

IN (3)

NWELL (2)

Configure Probe Net Lock

> \$choice=3

3

>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002/Inv-DMOS4/inv-DMOS4.oas'

Top cell name = 'INVERTER'

SPICE deck file = 'invX2.cir'

13. Using DMOS4 for the [inv.cir](#) Tutorial

4. Run the modified LVS script four times: #4/4

NetlistSchematicCross ReferenceLog

Circuits

INVERTER

Objects

INVERTER

Pins

Nets

Devices

NMOS

S ↔ D

D ↔ S

G

B

PMOS

S

D

G

B

Layout

INVERTER

\$2 / NMOS [L=0.25, N / NMOS [L=0.25, W=0.9]

VSS (1) VSS (2)

OUT (2) OUT (3)

IN (2) IN (3)

SUBSTRATE (1) SUBSTRATE (2)

\$1 / PMOS [L=0.25, P / PMOS [L=0.25, W=1.5]

VDD (1) OUT (3)

OUT (2) VDD (2)

IN (2) IN (3)

NWELL (1) NWELL (2)

Configure

Probe Net

☐ Lock

> \$choice=4

4

>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002/Inv-DMOS4/inv-DMOS4.oas'

Top cell name = 'INVERTER'

SPICE deck file = 'inv-DMOS4.cir'

```
1 |
2 * Simple CMOS inverter circuit
3 *
4 * Original: ${klayout_root}/testdata/lvs/inv.cir
5 *
6 * Modified: inv-DMOS4.cir (PMOS, NMOS)=( correct, correct) $choice=4
7 * by: Kazzz-S
8 * date: 2023-02-16
9 * aims: 1) correct D-S connections of the PMOS (flipped in the original)
10
11 .SUBCKT INVERTER VSS IN OUT NWELL SUBSTRATE VDD
12 * Mp VDD IN OUT NWELL PMOS W=1.5U L=0.25U
13 Mp OUT IN VDD NWELL PMOS W=1.5U L=0.25U
14 Mn OUT IN VSS SUBSTRATE NMOS W=0.9U L=0.25U
15 .ENDS
16
```

I expected this should match. But failed!

14. Using DMOS4 for a **2-input NAND**



WENSHIH

February 17

https://www.klayout.de/forum/discussion/comment/_9493

on 2023-02-17

Thanks for your suggestion and helps! If there is any information I can supply, please tell me.
Here is the test file.

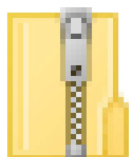


nand.test.zip
14.7K



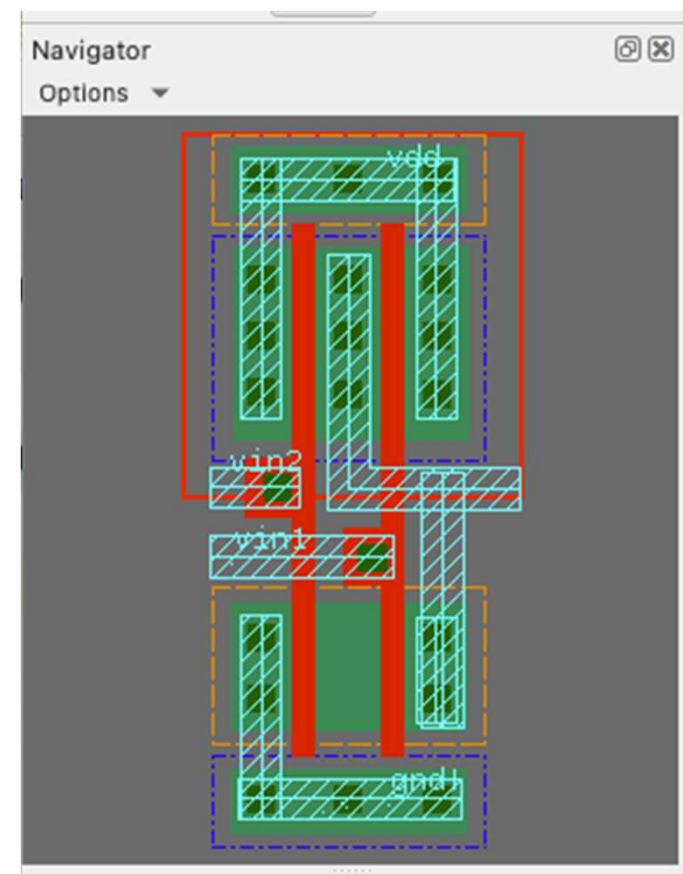
Starting point. Thank you for providing this!

1. Check the provided resource files and modify them if necessary.



All Files

NAND-DMOS4.zi
p



14. Using DMOS4 for a 2-input NAND

Cells

▼ nand

▶ M1_M5

▶ M1_M5\$1

▶ M1_M6

▶ M1_M6\$1

M1_V1_M2

M1_V1_M2\$1

M5_V5_M6

M5_V5_M6\$1

NCELL\$\$\$33500204

NCELL\$\$\$33500204\$1

NCELL\$\$\$33501228

NCELL\$\$\$33501228\$1

NCELL\$\$\$33504300

NCELL\$\$\$33504300\$1

PCELL\$\$\$33495084

PCELL\$\$\$33495084\$1

PCELL\$\$\$33496108

PCELL\$\$\$33496108\$1

PCELL\$\$\$33497132

PCELL\$\$\$33497132\$1

PCELL\$\$\$33498156

PCELL\$\$\$33498156\$1

PO_CO_M1

PO_CO_M1\$1

nimp_vdd_noCO

nimp_vdd_noCO\$1

npimp

npimp\$1

pimp_gnd_noCO

pimp_gnd_noCO\$1

Too many ghost cells

Levels 0 .. 3

→

Cells

▼ nand

▶ M1_M5

▶ M1_M5\$1

▶ M1_M6

▶ M1_M6\$1

M1_V1_M2

M1_V1_M2\$1

M5_V5_M6

M5_V5_M6\$1

NCELL\$\$\$33500204

NCELL\$\$\$33500204\$1

NCELL\$\$\$33501228

NCELL\$\$\$33501228\$1

NCELL\$\$\$33504300

NCELL\$\$\$33504300\$1

PCELL\$\$\$33495084

PCELL\$\$\$33495084\$1

PCELL\$\$\$33496108

PCELL\$\$\$33496108\$1

PCELL\$\$\$33497132

PCELL\$\$\$33497132\$1

PCELL\$\$\$33498156

PCELL\$\$\$33498156\$1

PO_CO_M1

PO_CO_M1\$1

nimp_vdd_noCO

nimp_vdd_noCO\$1

npimp

npimp\$1

pimp_gnd_noCO

pimp_gnd_noCO\$1

Levels 0 .. 1

→

Navigator

Options ▼



Cells

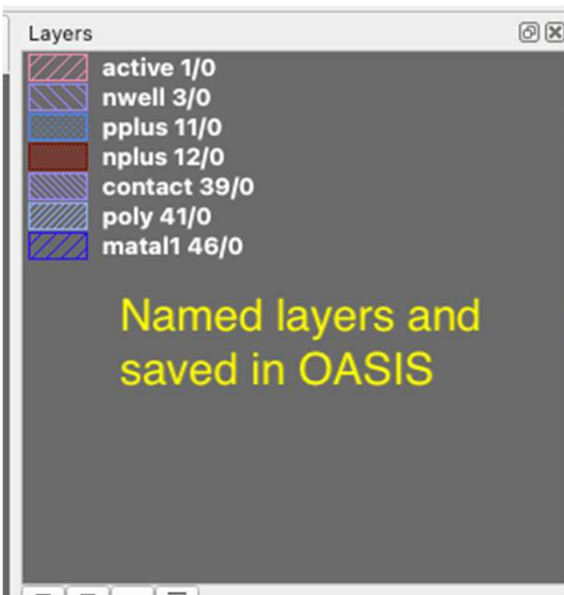
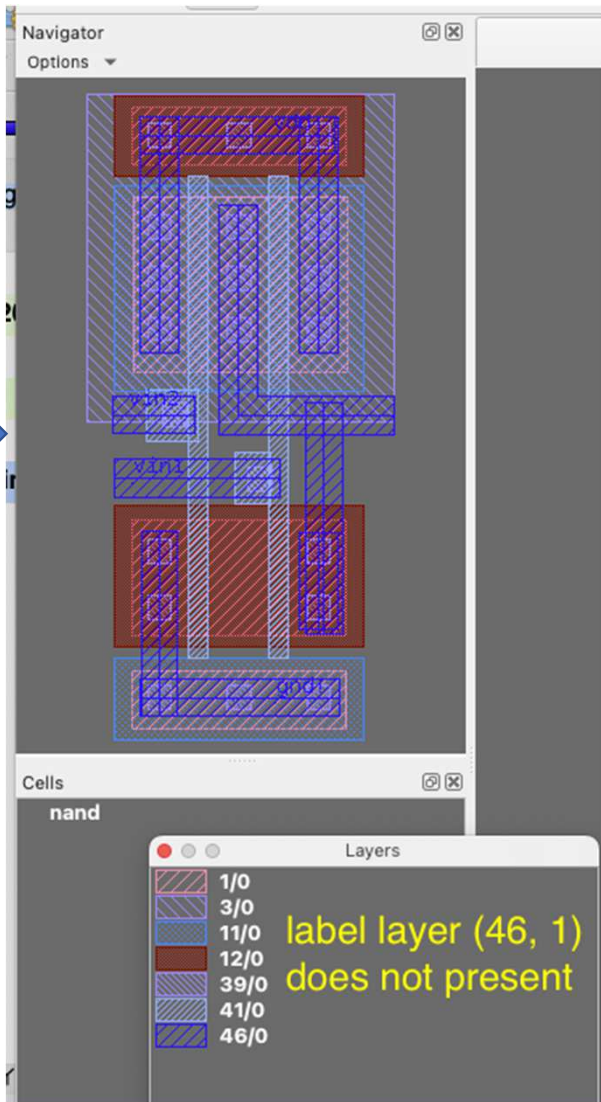
nand

KLayout Forum No. 2238 (as Study002: LVS of CMOS Inverter and 2-input NAND)

36

14. Using DMOS4 for a 2-input NAND

```
11 # Drawing layers:
12
13 poly = input(41, 0)
14 active = input(1, 0)
15 nwell = input(3, 0)
16 gate = poly & active
17 nplus = input(12, 0)
18 pplus = input(11, 0)
19 #nplus_od = nplus & active
20 #pplus_od = pplus & active
21 #nplus_od_nw = nplus & active & nwell
22 #pplus_od_nw = pplus & active & nwell
23 contact = input(39, 0)
24 metal1 = input(46, 0)
25 metal1_lbl = labels(46, 1)
26 via1 = input(47, 0)
27 metal2 = input(48, 0)
28 metal2_lbl = labels(48, 1)
29 via2 = input(49, 0)
30 metal3 = input(50, 0)
31 metal3_lbl = labels(50, 1)
32 # Bulk layer for terminal provisioning
33
```



14. Using DMOS4 for a 2-input NAND

2. Prepare two SPICE deck files.

```
nand.cir
1 .SUBCKT nand
2 M_M6 GND VIN2 N15943 GND MbreakN L=0.18um W=1.08um
3 M_M3 N15943 VIN1 VOUT GND MbreakN L=0.18um W=1.08um
4 M_M5 VDD VIN1 VOUT VDD MbreakP L=0.18um W=1.62um
5 M_M4 VDD VIN2 VOUT VDD MbreakP L=0.18um W=1.62um
6 .ENDS
7
```

terminals are missing

original SPICE deck

```
1 * https://www.klayout.de/forum/discussion/comment/9493/#Comment_9493
2 *
3 * Modified the original SPICE net
4 * 1) there is no tie-down diodes in the original layout
5 * 2) added terminals [VDD GND VIN1 VIN2 VOUT NWELL SUBSTRATE]
6 * 3) transistor name changed to the default (MbreakN, MbreakP) ==> (NMOS, PMOS)
7 * 4) Still INCORRECT! ==> Source-Drain interchanged
8
9 .SUBCKT nand VDD GND VIN1 VIN2 VOUT NWELL SUBSTRATE
10 M_M6 GND VIN2 N15943 SUBSTRATE NMOS L=0.18um W=1.08um
11 M_M3 N15943 VIN1 VOUT SUBSTRATE NMOS L=0.18um W=1.08um
12 M_M5 VDD VIN1 VOUT NWELL PMOS L=0.18um W=1.62um
13 M_M4 VDD VIN2 VOUT NWELL PMOS L=0.18um W=1.62um
14 .ENDS
```

\$choice=1 nand-incorrect.cir

D and S are swapped

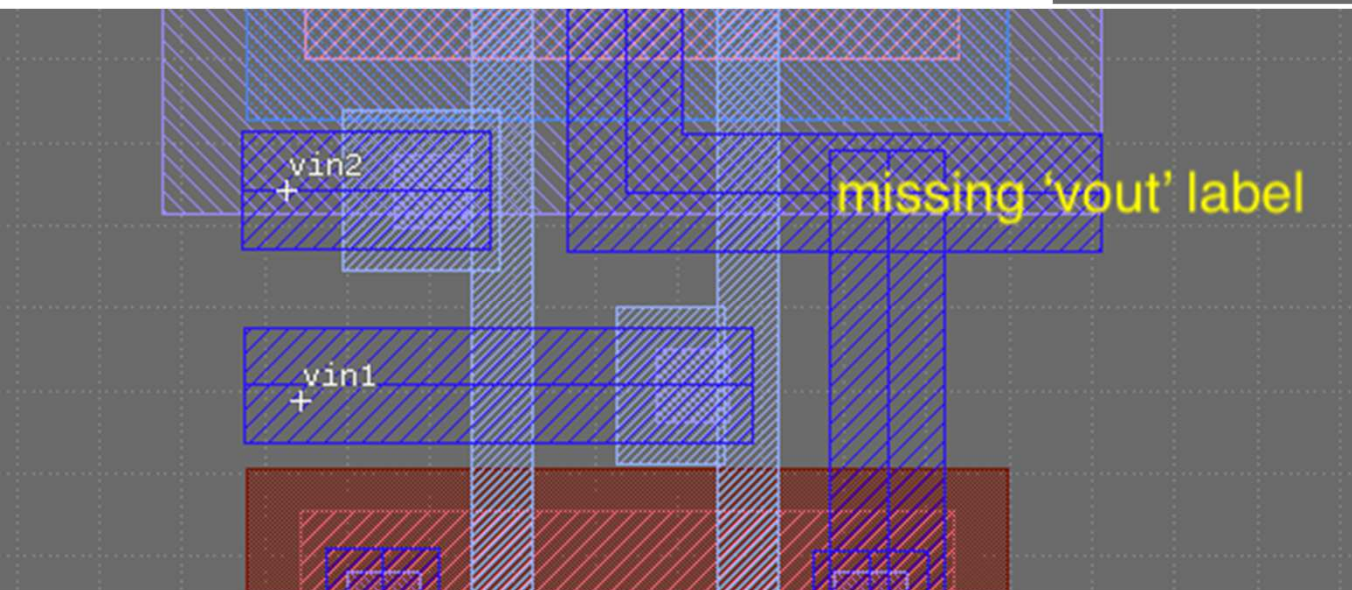
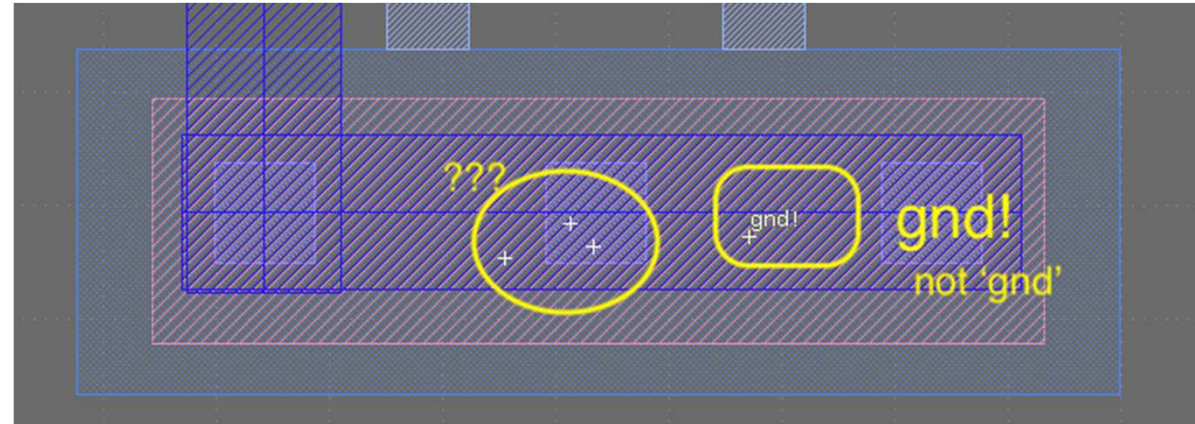
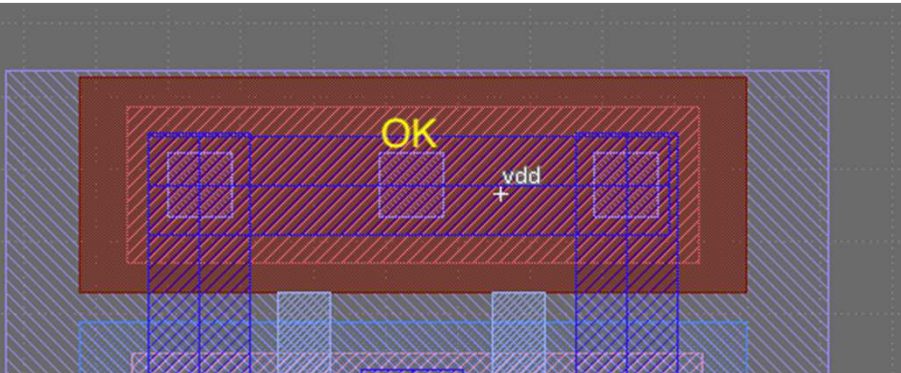
```
1 * https://www.klayout.de/forum/discussion/comment/9493/#Comment_9493
2 *
3 * Modified the original SPICE net
4 * 1) there is no tie-down diodes in the original layout
5 * 2) added terminals [VDD GND IN1 IN2 OUT NWELL SUBSTRATE]
6 * 3) transistor name changed to the default (MbreakN, MbreakP) ==> (NMOS, PMOS)
7 * 4) S-D connections are !CORRECT!
8
9 .SUBCKT nand VDD GND IN1 IN2 OUT NWELL SUBSTRATE
10 M_M6 N15943 VIN2 GND SUBSTRATE NMOS L=0.18um W=1.08um
11 M_M3 OUT VIN1 N15943 SUBSTRATE NMOS L=0.18um W=1.08um
12 M_M5 OUT VIN1 VDD NWELL PMOS L=0.18um W=1.62um
13 M_M4 OUT VIN2 VDD NWELL PMOS L=0.18um W=1.62um
14 .ENDS
```

\$choice=4 nand.cir

I expect this should match!

14. Using DMOS4 for a **2-input NAND**

3. Check the original design in GDS2.

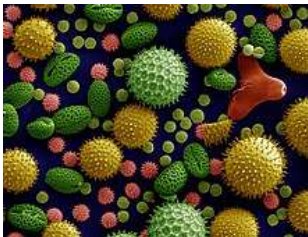


14. Using DMOS4 for a 2-input NAND

4. Prepare my design in OASIS:
"nand-DMOS4.oas"

Monoecy (/məˈniːsi/;
adj. **monoecious** /məˈniːʃəs/)^[1] is
a sexual system in seed
plants where
separate male and female cones
or flowers are present on the same
plant.

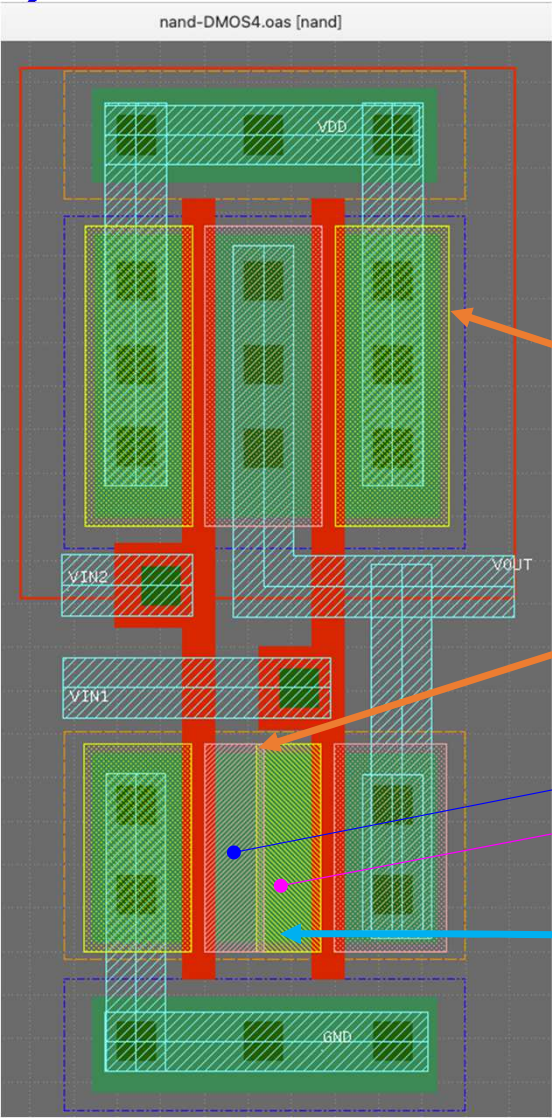
[Monoecy - Wikipedia](#)



[Pollen - Wikipedia](#)



Pollen can be
seen as the
majority carrier.



Added some
helper layers
for
experiments

Layers	
active	1/0
nwell	3/0
pplus	11/0
nplus	12/0
poly	41/0
contact	39/0
metal1	46/0
metal1_lbs	46/1
S-Recognition	51/0
MaleS-Recognition	51/1
D-Recognition	52/0
FemaleD-Recognition	52/1

Drain ♀

Source ♂

monoecious
plant

14. Using DMOS4 for a 2-input NAND

5. Modify the LVS script for testing and debugging.

```
136 nss
137 nnd
138 nsmale
139 ndfemale
140
141 #-----
142 # [3] Drawing layers
143 #-----
144 # [5] Device extraction
145 # PMOS (with ordinary
146 extract_devices(dmos4
147
148 # NMOS (with ordinary
149 extract_devices(dmos4
150
151 # NMOS (with female D
152 extract_devices(dmos4
153
154 # NMOS (with male S)
155 extract_devices(dmos4
156
157 # NMOS (with female D
158 extract_devices(dmos4
159
160 #-----
161 # [4] Computed layers
162 #-----
163 # [6] Define connecti
164 #-----
165 # Inter-layer
166 connect(pss,
167 connect(pdd,
168 connect(nss,
169 connect(ndd,
170 connect(poly,
171 connect(contact,
172 connect(metall,
173 connect(nsmale,
174
175 # Global
176 #connect_global(bulk,
177 #connect_global(ptie,
178 connect_global(bulk,
179 connect_global(nwell, "NELL")
180
181 #-----
182 # [7] Com
183 #-----
184 schematic
185
186 compare
187
188 # EOF
189
```

```
91
92
93 #-----
94 # [3] Drawing layers
95 #-----
96 active = input(1, 0)
97 nwell = input(3, 0)
98 pplus = input(11, 0)
99 nplus = input(12, 0)
100 poly = input(41, 0)
101 contact = input(39, 0)
102 metall = input(46, 0)
103 metall_lbl = labels(46, 1)
104 source_rec = input(51, 0) # not realis
105 drain_rec = input(52, 0) # not realis
106
107 # More helper layers to virtually disti
108 # of a "monoecious plant" (extracted as
109 # I call them "male source" and "female
110 male_S_rec = input(51, 1) # helper lay
111 female_D_rec = input(52, 1) # helper lay
112
113 # Bulk layer for terminal provisioning
114 bulk = polygon_layer
115
116 #-----
117 # [4] Computed layers
118 #-----
119 # In a future "nand-DMOS4B.lvs", we will
120 # to use the S- and D-recognition helper
121 #-----
122 #-----
123 active_in_nwell = active & nwell
124 pactive = active in nwell & pp
125 pgate = pactive & poly
126 psd = pactive - pgate
127 #ntie = active in nwell & n
128 pss = psd & source_rec
129 pdd = psd & drain_rec
130
131 active_outside_nwell = active - nwell
132 nactive = active outside_nwell
133 ngate = nactive & poly
134 nsd = nactive - ngate
135 #ptie = active_outside_nwell & pplus
136
```

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```

```
1
2 # Original: "lvs 2 1.lylvs" in the attached ZIP file of
3 # https://www.klayout.de/forum/discussion/comment/9493/#Comment_9493
4
5 # Modified: nand-DMOS4A.lvs
6 # by: Kazzz-S
7 # date: 2023-02-21
8 # aims: 1) test WENSHIH's NAND circuit with two SPICE decks: INCORRECT(original) & CORRECT
9 # 2) use "DMOS4" instead of "MOS4"
10 # ==> https://www.klayout.de/forum/discussion/comment/9484/#Comment_9484
11 # 3) use "helper layers" for source- and drain-recognition
12
13 #-----
14 # [0] Utilities
15
16
17 def AboutCurrentDesign(spicedeck)
18     designFile = RBA::CellView::active.filename
19     activeLayout = RBA::CellView::active.layout
20     puts ">>> Current design file = '#{designFile}'"
21     puts "    Top cell name = '#{activeLayout.top_cell.name}'"
22     puts "    SPICE deck file = '#{spicedeck}'"
23 end
24
25 class SpiceDeckSelector
26     def initialize
27         if $choice == nil # global variable to choose a SPICE deck
28             $choice = 10
29         end
30         @spicedeck = [ $choice, "" ]
31
32         @spiceOpt = { 0 => "exit", 1 => "original", 4 => "correct" }
33         @spiceDECK = { "original" => "nand-incorrect.cir", # (PMOS, NMOS)=(incorrect, incorrect)
34                       "correct" => "nand.cir" # (PMOS, NMOS)=( correct, correct)
35         }
36     end
37
38     def GetSpiceDeck
39         return @spicedeck
40     end
41
42     def GetOneOption
43         case $choice
44         when 0
45             puts "Bye! You can ignore the exception if caught."
46         end
47     end
48
49 # [2] Reports
50
51 # Store the LVS report to this file
52 report_lvs( "nand-DMOS4A-choice#{choice}.lvldb", true )
53
54 # Write the extracted netlist to this file
55 target_netlist( "nand-DMOS4A-choice#{choice}_extracted.cir",
56                 write_spice,
57                 "Extracted by KLayout with <#{spicedeck}>" )
58
```

nand-DMOS4A.lvs

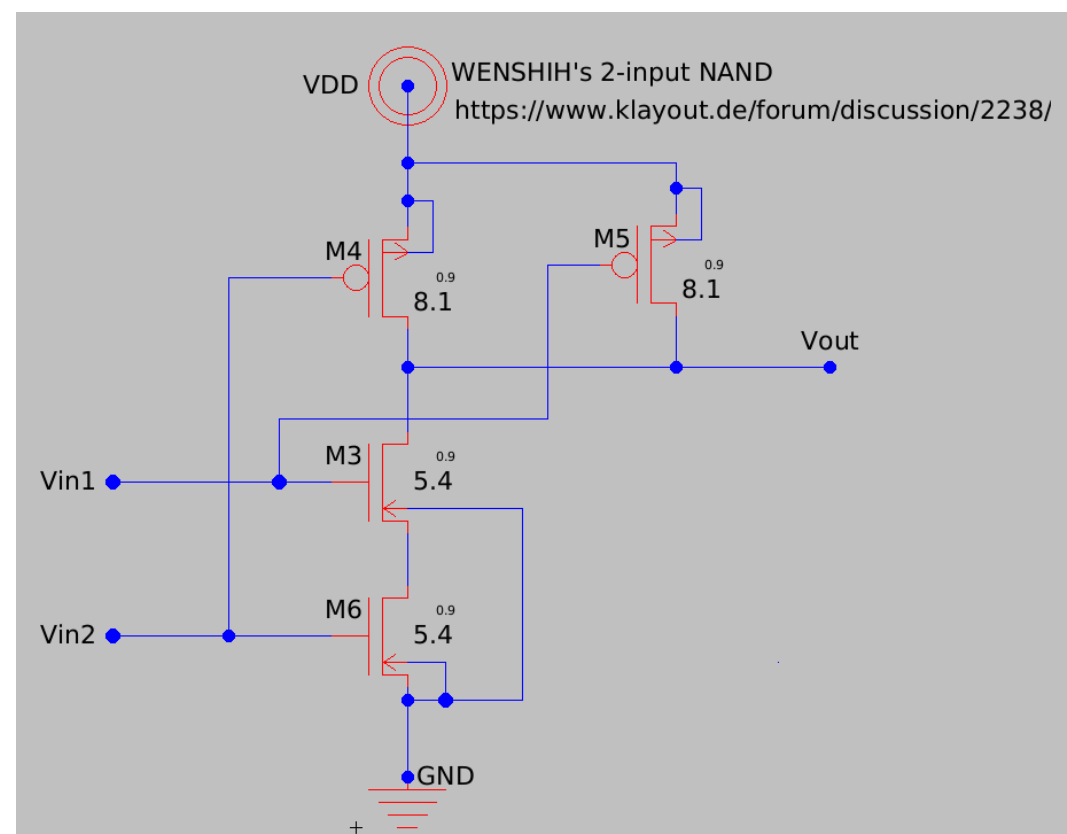
14. Using DMOS4 for a 2-input NAND

6. Run the modified LVS script twice: #1/2

The screenshot shows the KLayout software interface. On the left, the 'Circuits' pane displays a hierarchical view of the layout, including VDD, GND, VIN1, VIN2, VOUT, and transistors M3, M4, M5, and M6. The main area shows the layout of the NAND gate with these components. On the right, the 'Objects' pane lists the devices and their properties, including NMOS and PMOS transistors with their respective parameters (L, W, S, D, G, B). At the bottom, the command line shows the execution of the LVS script, with the output indicating the current design file, top cell name, and SPICE deck file.

```
1 * https://www.klayout.de/forum/discussion/comment/9493/#Comment_9493
2 *
3 * Modified the original SPICE net
4 * 1) there is no tie-down diodes in the original layout
5 * 2) added terminals [VDD GND VIN1 VIN2 VOUT NWELL SUBSTRATE]
6 * 3) transistor name changed to the default (MbreakN, MbreakP) ==> (NMOS, PMOS)
7 * 4) Still INCORRECT! ==> Source-Drain interchanged
8 *
9 .SUBCKT nand VDD GND VIN1 VIN2 VOUT NWELL SUBSTRATE
10 M M6 GND VIN2 N15943 SUBSTRATE NMOS L=0.18um W=1.08um
11 M M3 N15943 VIN1 VOUT SUBSTRATE NMOS L=0.18um W=1.08um
12 M M5 VDD VIN1 VOUT NWELL PMOS L=0.18um W=1.62um
13 M M4 VDD VIN2 VOUT NWELL PMOS L=0.18um W=1.62um
14 .ENDS
```

\$choice=1
This matched!



14. Using DMOS4 for a 2-input NAND

6. Run the modified LVS script twice: #2/2

The screenshot shows the KLayout LVS tool interface. On the left is a layout view of a 2-input NAND gate with transistors M4, M5, M6, and M3. The layout includes VDD and GND rails. On the right is the netlist view, which lists the devices and their connections. The netlist shows two NMOS transistors (M4 and M5) and two PMOS transistors (M6 and M3). The connections are as follows:

- Device M4 (NMOS):** S to GND (1), D to \$6 (2), G to VIN2 (2), B to SUBSTRATE (2).
- Device M5 (NMOS):** S to \$3 (2), D to VOUT (3), G to VIN1 (2), B to SUBSTRATE (2).
- Device M6 (PMOS):** S to VDD (2), D to VOUT (3), G to VIN1 (2), B to NWELL (2).
- Device M3 (PMOS):** S to VDD (2), D to VOUT (3), G to VIN2 (2), B to NWELL (2).

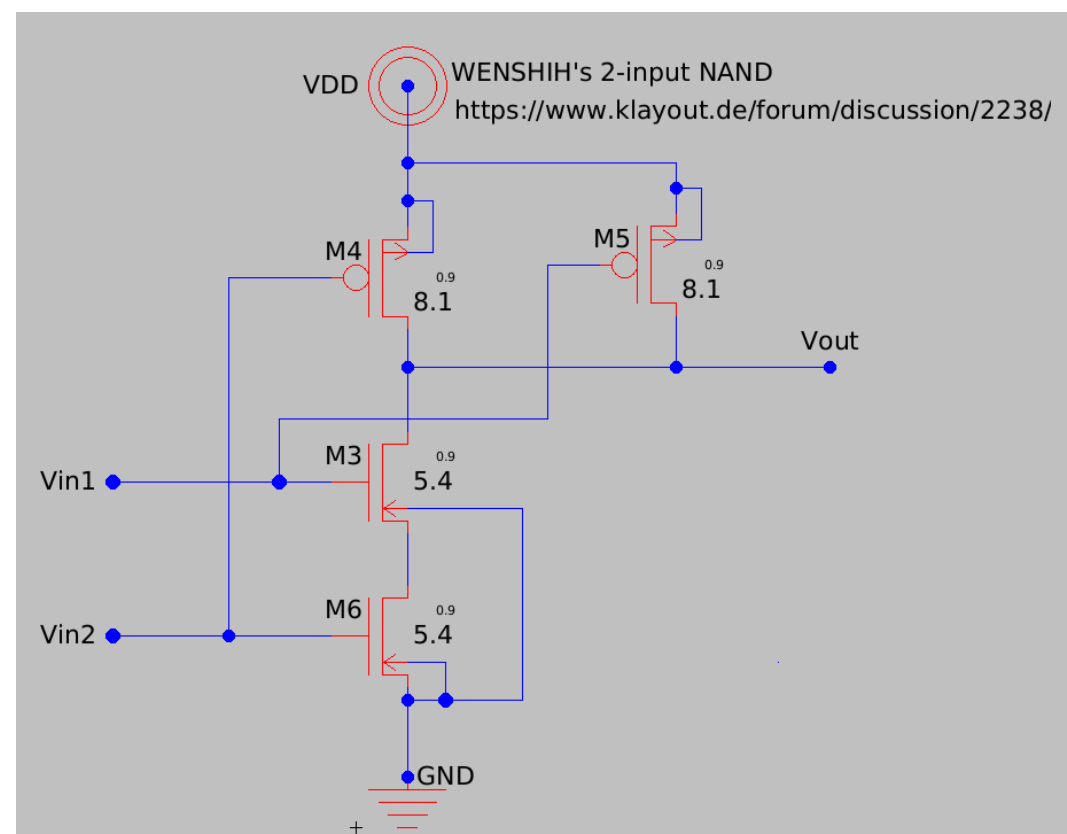
At the bottom, the command prompt shows the execution of the LVS script:

```
> $choice=4
4
>>> Current design file = '/home/sekigawa/GitWork/ForumKLayout/Study002/NAND-DMOS4/nand-DMOS4.oas'
Top cell name = 'nand'
SPICE deck file = 'nand.cir'
```

```
1 * https://www.klayout.de/forum/discussion/comment/9493/#Comment_9493
2 *
3 * Modified the original SPICE net
4 * 1) there is no tie-down diodes in the original layout
5 * 2) added terminals [VDD GND IN1 IN2 OUT NWELL SUBSTRATE]
6 * 3) transistor name changed to the default (MbreakN, MbreakP) ==> (NMOS, PMOS)
7 * 4) S-D connections are !CORRECT!
8
9 .SUBCKT nand VDD GND IN1 IN2 OUT NWELL SUBSTRATE
10 M M6 N15943 VIN2 GND SUBSTRATE NMOS L=0.18um W=1.08um
11 M M3 OUT VIN1 N15943 SUBSTRATE NMOS L=0.18um W=1.08um
12 M M5 OUT VIN1 VDD NWELL PMOS L=0.18um W=1.62um
13 M M4 OUT VIN2 VDD NWELL PMOS L=0.18um W=1.62um
14 .ENDS
```

\$choice=4

I expected this should match. But failed!



15. Summary and Intermediate Conclusions as of 2023-02-20

- ◆ To use **DMOS4** in LVS, I employed the notion of an **extraction helper layer**.
 - I'm not sure if **inv-DMOS4A.lvs** and **nand-DMOS4A.lvs** are appropriate or not.
 - Any suggestion will be highly appreciated.
- ◆ The **net extracted from a layout is correct** (in the two cases).
- ◆ However, a **reference net (SPICE deck) seems to be misinterpreted...**
 - as if S and D are **always (forcibly) swapped first** even if the intention is...

The way I implement swapping is that for "MOS3" and "MOS4" **I treat the schematic netlist as given** (even if drain is on VDD or GND) and try both ways of the extracted device until a match is found. For "DMOS3" and "DMOS4" the latter step is skipped.



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